AMD AM4 B550

M-ATX (243.84 X 243.84)

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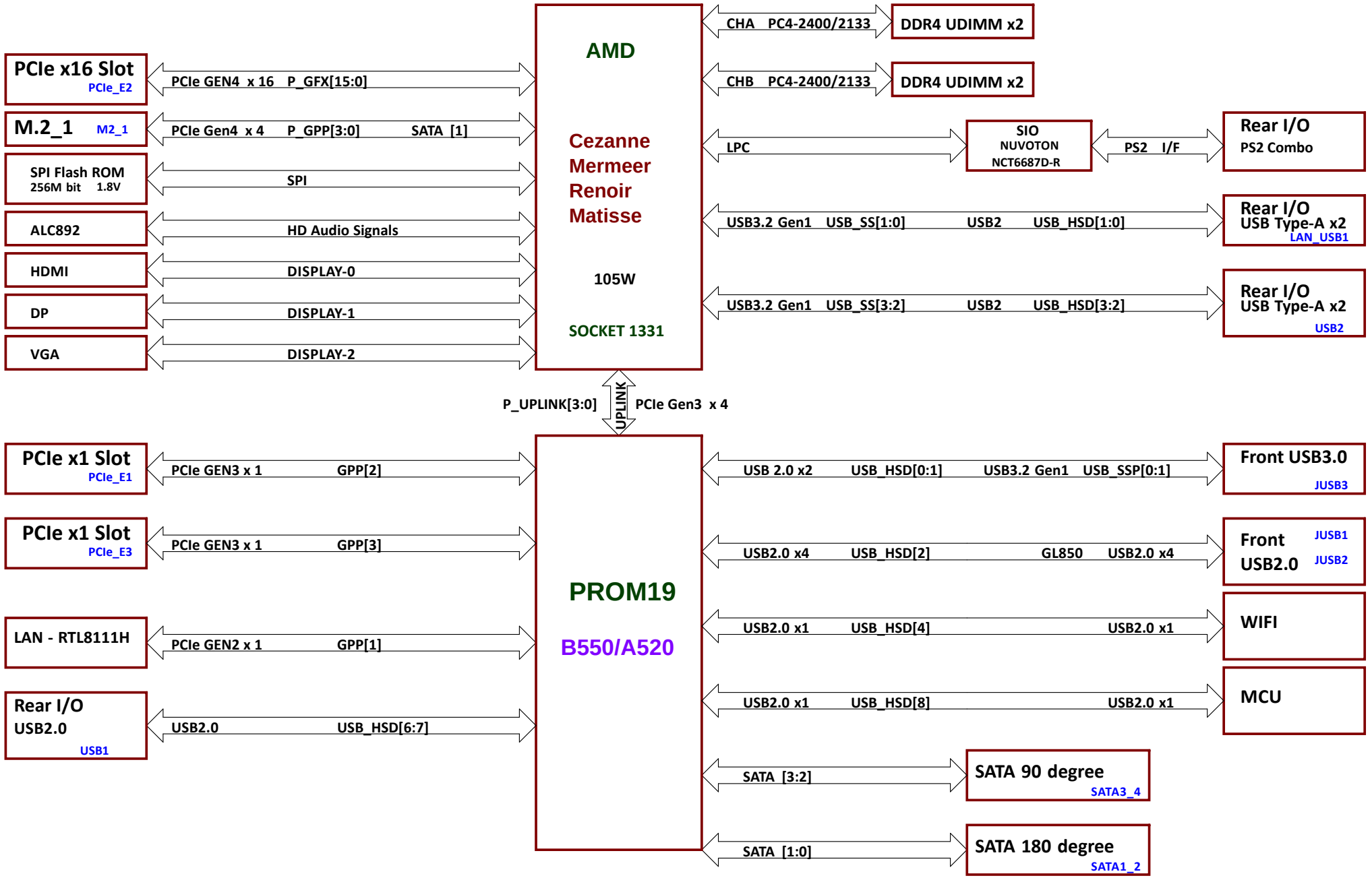

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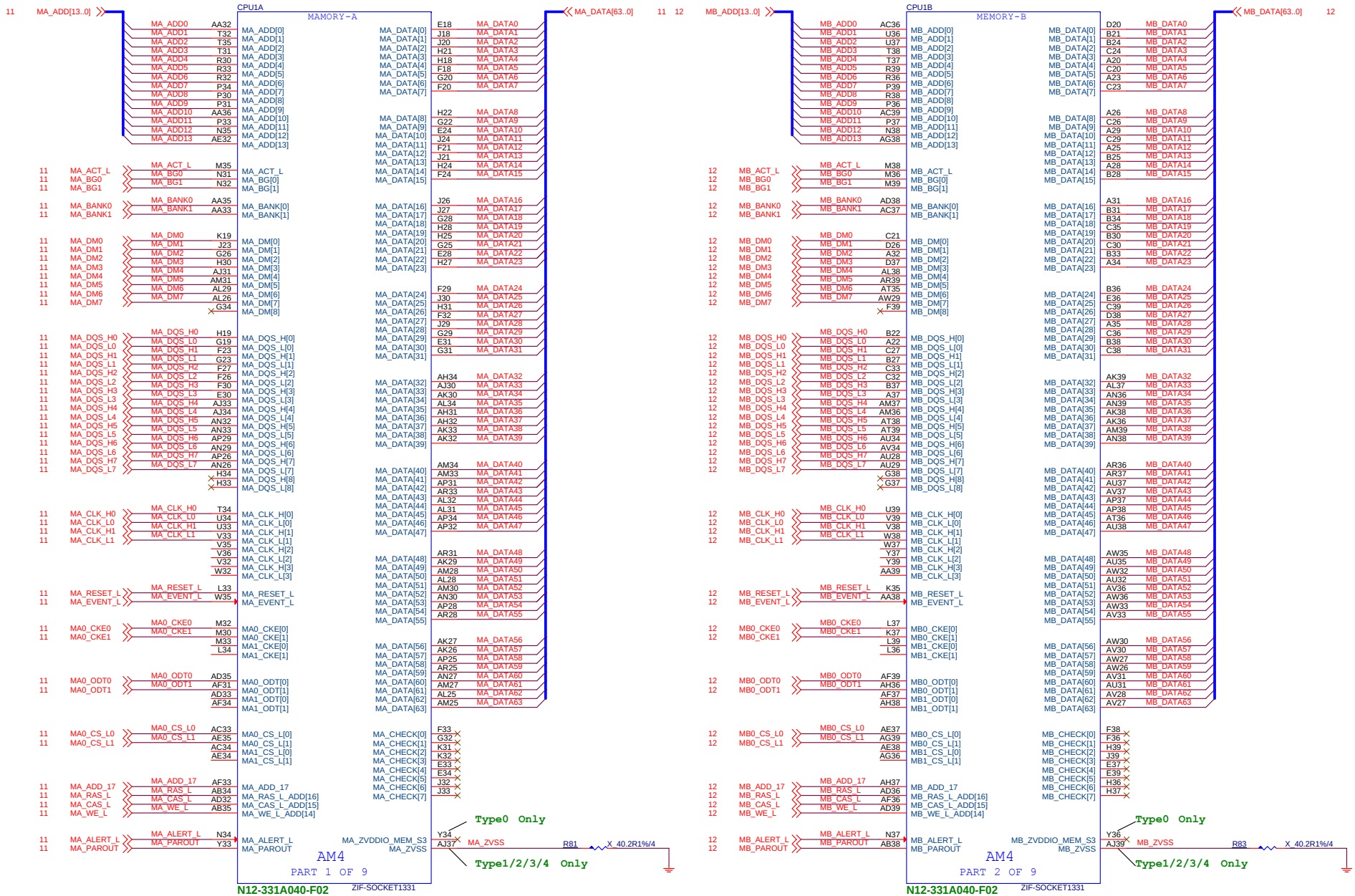

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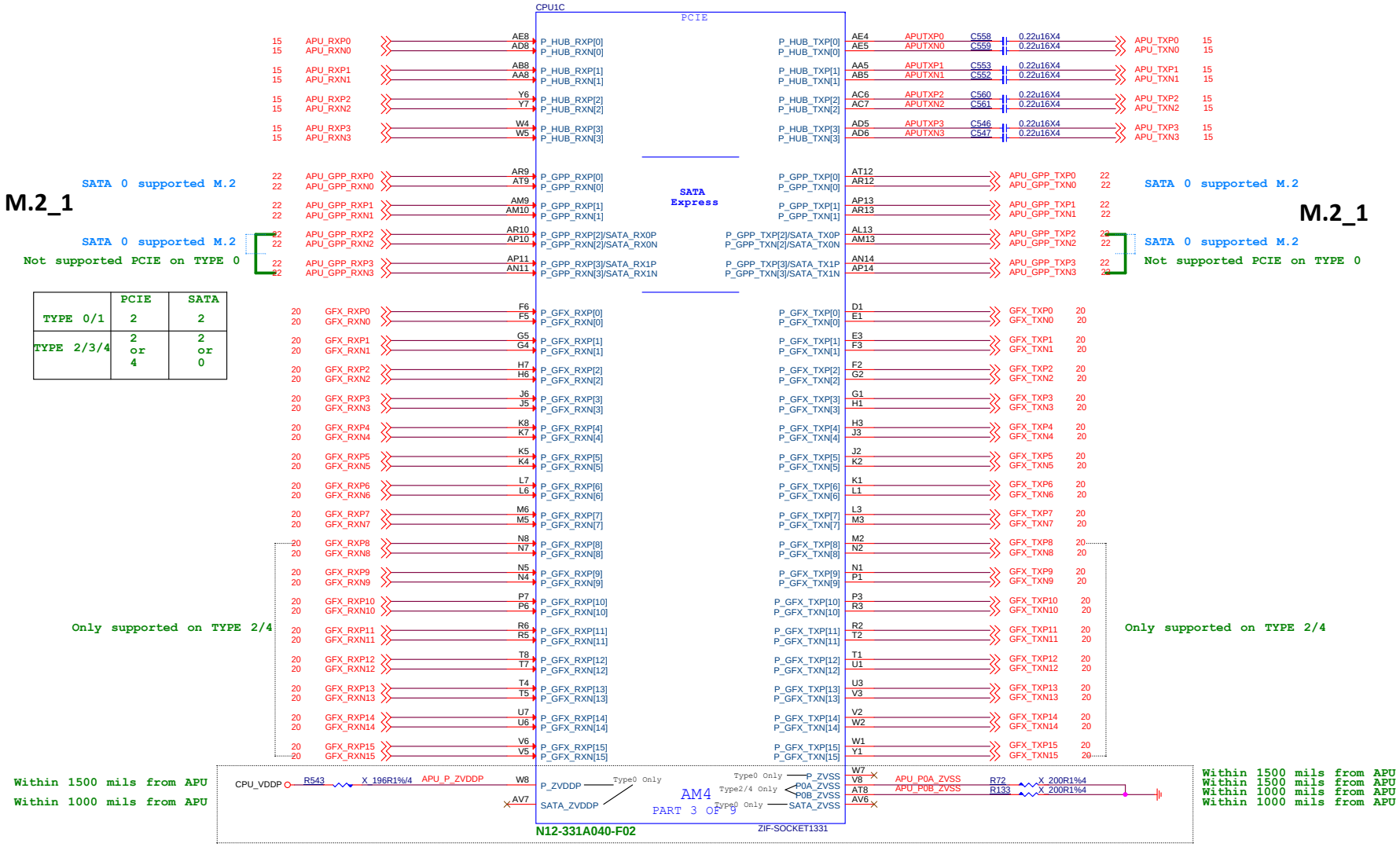

	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

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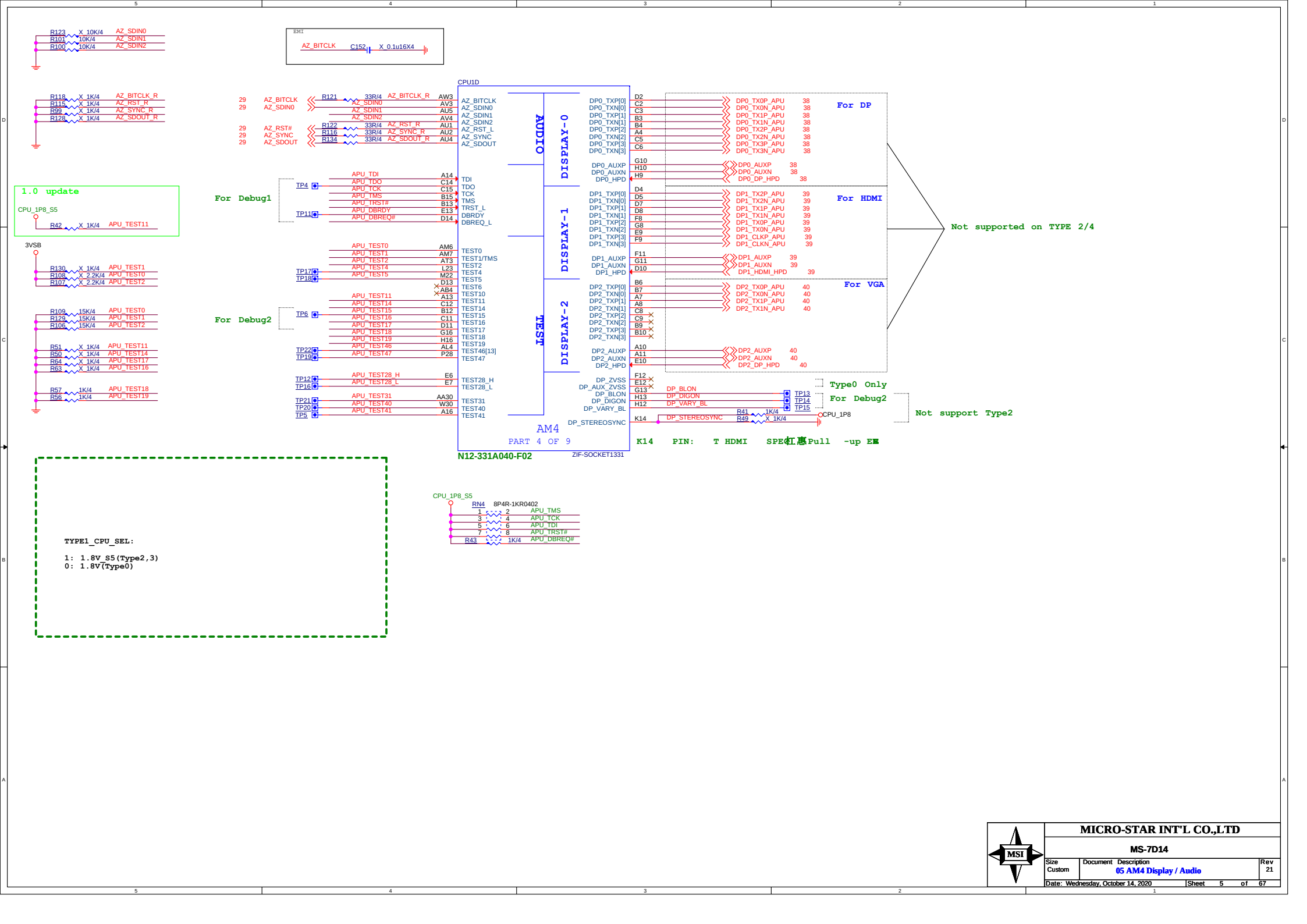
R123 X_10K/4 AZ_SDIN0
R101 10K/4 AZ_SDIN1
R100 10K/4 AZ_SDIN2
EMI
AZ_BITCLK C152 X_0.1u16X4
R118 X_1K/4 AZ_BITCLK_R
R115 X_1K/4 AZ_RST_R
R99 X_1K/4 AZ_SYNC_R
R128 X_1K/4 AZ_SDOUT_R
29 AZ_BITCLK
29 AZ_SDIN0
R121 33R/4 AZ_BITCLK_R
AZ_SDIN0
AZ_SDIN1
AZ_SDIN2
29 AZ_RST#
29 AZ_SYNC
29 AZ_SDOUT
R122 33R/4 AZ_RST_R
R116 33R/4 AZ_SYNC_R
R134 33R/4 AZ_SDOUT_R
CPU1D
AZ_BITCLK AW3
AZ_SDIN0 AV3
AZ_SDIN1 AU5
AZ_SDIN2 AV4
AZ_RST_L AU1
AZ_SYNC AU2
AZ_SDOUT AU4
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
DP0_TXP[0] D2
DP0_TXN[0] C2
DP0_TXP[1] C3
DP0_TXN[1] B3
DP0_TXP[2] B4
DP0_TXN[2] A4
DP0_TXP[3] C5
DP0_TXN[3] C6
DP0_AUXP G10
DP0_AUXN H10
DP0_HPD H9
DP0_TX0P_APU 38
DP0_TX0N_APU 38
DP0_TX1P_APU 38
DP0_TX1N_APU 38
DP0_TX2P_APU 38
DP0_TX2N_APU 38
DP0_TX3P_APU 38
DP0_TX3N_APU 38
DP0_AUXP 38
DP0_AUXN 38
DP0_DP_HPD 38
For DP
DP1_TXP[0] D4
DP1_TXN[0] D5
DP1_TXP[1] D7
DP1_TXN[1] D8
DP1_TXP[2] F8
DP1_TXN[2] G8
DP1_TXP[3] E9
DP1_TXN[3] F9
DP1_AUXP F11
DP1_AUXN G11
DP1_HPD D10
DP1_TX2P_APU 39
DP1_TX2N_APU 39
DP1_TX1P_APU 39
DP1_TX1N_APU 39
DP1_TX0P_APU 39
DP1_TX0N_APU 39
DP1_CLKP_APU 39
DP1_CLKN_APU 39
DP1_AUXP 39
DP1_AUXN 39
DP1_HDMI_HPD 39
For HDMI
DP2_TXP[0] B6
DP2_TXN[0] B7
DP2_TXP[1] A7
DP2_TXN[1] A8
DP2_TXP[2] C8
DP2_TXN[2] C9
DP2_TXP[3] B9
DP2_TXN[3] B10
DP2_AUXP A10
DP2_AUXN A11
DP2_HPD E10
DP2_TX0P_APU 40
DP2_TX0N_APU 40
DP2_TX1P_APU 40
DP2_TX1N_APU 40
DP2_AUXP 40
DP2_AUXN 40
DP2_DP_HPD 40
For VGA
Not supported on TYPE 2/4
DP_ZVSS F12
DP_AUX_ZVSS E12
DP_BLON G13
DP_DIGON H13
DP_VARY_BL H12
DP_STEREOSYNC K14
DP_BLON
DP_DIGON
DP_VARY_BL
DP_STEREOSYNC
TP13
TP14
TP15
Type0 Only
For Debug2
Not support Type2
R41 1K/4
R49 X_1K/4
CPU_1P8
K14 PIN: T HDMI SPEC建議Pull -up 3K
TP4
TP11
APU_TDI A14
APU_TDO C14
APU_TCK C15
APU_TMS B15
APU_TRST# B13
APU_DBRDY E13
APU_DBREQ# D14
TDI
TDO
TCK
TMS
TRST_L
DBRDY
DBREQ_L
For Debug1
1.0 update
CPU_1P8_S5
R42 X_1K/4 APU_TEST11
3VSB
R130 X_1K/4 APU_TEST1
R108 X_2.2K/4 APU_TEST0
R107 X_2.2K/4 APU_TEST2
TP17
TP18
APU_TEST0 AM6
APU_TEST1 AM7
APU_TEST2 AT3
APU_TEST4 L23
APU_TEST5 M22
D13
AB4
A13
TEST0
TEST1/TMS
TEST2
TEST4
TEST5
TEST6
TEST10
TEST11
TEST14
TEST15
TEST16
TEST17
TEST18
TEST19
TEST46[13]
TEST47
R109 15K/4 APU_TEST0
R129 15K/4 APU_TEST1
R106 15K/4 APU_TEST2
R51 X_1K/4 APU_TEST11
R50 X_1K/4 APU_TEST14
R64 X_1K/4 APU_TEST17
R63 X_1K/4 APU_TEST16
R57 1K/4 APU_TEST18
R56 1K/4 APU_TEST19
TP6
TP22
TP19
APU_TEST11
APU_TEST14 C12
APU_TEST15 B12
APU_TEST16 C11
APU_TEST17 D11
APU_TEST18 G16
APU_TEST19 H16
APU_TEST46 AL4
APU_TEST47 P28
TP12
TP16
APU_TEST28_H E6
APU_TEST28_L E7
TEST28_H
TEST28_L
TP21
TP20
TP5
APU_TEST31 AA30
APU_TEST40 W30
APU_TEST41 A16
TEST31
TEST40
TEST41
AM4
PART 4 OF 9
N12-331A040-F02
ZIF-SOCKET1331
CPU_1P8_S5
RN4 8P4R-1KR0402
1 2 APU_TMS
3 4 APU_TCK
5 6 APU_TDI
7 8 APU_TRST#
R43 1K/4 APU_DBREQ#
TYPE1_CPU_SEL:
1: 1.8V_S5(Type2,3)
0: 1.8V(Type0)
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1.0 update FIX SMBUS PK-PK issue

Closed FAN , by S0ix.

24,26,27 FAN_EN
CPU_S0_IDLE
Q18 X_2N7002
R224 X_100K/4

24,38,46,48,49,51,55 SLP_S3#
3VSB
C148 0.1u16X4
U11
R126 100K/4
APU_S0A3_GPIO
APU_SLP_S3#
R104 2.2K/4
R103 100K/4
AHCT1G126GV_SOT23-5-RH
APU_SLP_S3#
1:See APU_S0A3_GPIO
0:High-IMpedance
T33-1G12629-T07
AVL:T33-1G12619-N78

SLP_S3# R125 X_0R/4 APU_SLP_S3#

3VSB R265 X_10K/4
Q22 X_2N7002D
CHIP_PWGD 24,48,59
+12V R253 X_2.7K/4
C265 X_0.1u16X4
Q19 X_2N7002
Q20 X_2N7002
SCLK0_3VSB 58
SCLK0 6,11,53
SDATA0_3VSB 58
SDATA0 6,11,53

SCLK0_R R176 4.7K/4
SDATA0_R R182 4.7K/4
SCLK0_3VSB R245 X_4.7K/4
SDATA0_3VSB R246 X_4.7K/4
SCLK1 R92 2.2K/4
SDATA1 R93 2.2K/4
PE2_PE3_WAKE# R539 10K/4
PEGX16_WAKE# R541 10K/4
M2_PE4_WAKE# R540 10K/4
LAN_WAKE# R95 10K/4

VCC3
R53 1K/4 APU_ALERT#
R37 1K/4 APU_PROCHOT#
R58 1K/4 APU_THERMTRIP#

CPU_1P8
Within 500mils
R39 1K/4 APU_SIC
R40 1K/4 APU_SID
R52 300R/4 PWROK
R54 300R/4 RESET_L
Follow CRB

3VSB
R127 10K/4 PWRBTN#
R146 X_10K/4 APU_AM4R1
R137 10K/4 BLINK
R124 10K/4 APU_WAKE#
R112 10K/4 PCIE_RST
C145 100p50N4 PCIE_REST#

CPU_1P8_S5A
R138 22K/4 RSMRST#
C538 10u6.3X6
C156 0.1u16X4

C39 X_0.1u16X4 APU_PWROK
穩 獅 Qogir_Re ゥ 穩 糟 ㄗ叫 簡痙、ン

3VSB
C167 X_0.1u16X4
Level 3.3V U13
23 WIFI_BT_RTCCLK
RTCCLK
MC74VHC1GT50DFT1G_SC70-5-RH

For Moderm Standby Fail Use 1.0 update
APU_WAKE# R548 X_0R/4 PE2_PE3_WAKE# R542 0R/4 PE2_PE3_WK# 21,23
APU_WAKE# R194 X_0R/4 PEGX16_WAKE# R193 0R/4 PEGX16_WK# 20
APU_WAKE# R163 X_0R/4 LAN_WAKE# R162 0R/4 LAN_WK# 28

CPU1E

41 APU_SVC	D17 SVC	SVI	SMBus
41 APU_SVD	C17 SVD		
41 APU_SVT	A17 SVT		
41 APU_PWROK	R44 X_R/2 PWROK E16	ACPI	GPIO
48 ALL_PWR_PWRGD	AM3 PWR_GOOD		
	KBRST# D3 RESET_L B16		
24,41 APU_PROCHOT#	H15 PROCHOT_L		
APU_THERMTRIP#	A19 THERMTRIP_L		
0B update 20200313			
APU_SLP_S3#	AT2 SLP_S3_L		
24,49,51,55 SLP_S5#	R164 X_R/2 SLP_S5# R AP2		
APU_S0A3_GPIO	AR3 S0A3_GPIO/AGPIO10/SGPIO0_CLK		
S5_MUX_CTRL	TP24 AP4 S5_MUX_CTRL/EGPIO42		
24 PWRBTN#	AN5 PWR_BTN_L/AGPIO0		
BLINK	AT5 BLINK/AGPIO11		
56 SPKR	AW23 SPKR/AGPIO91		
24,48 RSMRST#	AP5 RSMRST_L		
7,48,52,56 SYSREST#	AM4 SYS_RESET_L/AGPIO1		
7,17,20,22,23,28 PCIE_REST#	R119 33R/4 PCIE_RST AL7 PCIE_RST_L/EGPIO26		
24 KBRST#	AN24 ESPI_RESET_L/KBRST_L		
17,22 APU_WAKE#	AL5 WAKE_L/AGPIO2		
17,24 APU_LPC_PME#	AL2 LPC_PME_L/AGPIO22		
24 APU_SIC	B18 SIC		
24 APU_SID	C18 SID		
APU_ALERT#	D16 ALERT_L		
Turn off power when BIOS into deep mode			
47,49,55 APU_AM4R1	AL8 AM4R1		
CORETYPE0	AM24 CORETYPE[0]		
CORETYPE1	AN9 CORETYPE[1]		
24,55 DEEP_S5	Q50 2N7002		
TP26 AGPIO84	AN23 FANIN0/AGPIO84	FAN	OC
	AP23 FANOUT0/AGPIO85		
Level 1.8V S5 Domain			
7 RTCCLK	AP8 RTCCLK	RTC	SENSE
APU_32K_X1	AW5 X32K_X1		
APU_32K_X2	AW6 X32K_X2		

AM4
PART 5 OF 9
N12-331A040-F02
ZIF-SOCKET1331

SCL0/I2C2_SCL/EGPIO113
SDA0/I2C2_SDA/EGPIO114
AU25 SCLK0_R R175 X_R/2 R218 X_0R/4 SIO_SMB_MSCL 24,40,41
AV25 SDATA0_R R175 X_R/2 R219 X_0R/4 SIO_SMB_MSDA 24,40,41
SCL1/I2C3_SCL/AGPIO19
SDA1/I2C3_SDA/AGPIO20
AK3 SCLK1 20
AK2 SDATA1 20
SCLK0 6,11,53
SDATA0 6,11,53

AGPIO3 AT6 PE2_PE3_WAKE#
AGPIO4 AR6 M2_1_SATA_DET 22
AGPIO5/DEVSLP0 AP22 DEVSLP1 22
AGPIO6 AR8 CPU_S0_IDLE
AGPIO8 AP7 LAN_ISOLATEB 28
AGPIO9/SGPIO0_DATAOUT AN2 AGPIO9
AGPIO23/SGPIO0_LOAD AN3 PEGX16_WAKE#
AGPIO40/SGPIO0_DATAIN AR4 M22_PE4_WAKE#
AGPIO86 AW17
GENINT1_L/AGPIO89 AV22 GENINT1_L M2_1_CARD_DET 22
GENINT2_L/AGPIO90 AU23
SATA_ACT_L/AGPIO130 AM22 SATA_LED# 56

For Select Auto or Manual
VCC3
R148 8.2K/4 GENINT1_L
R139 X_10K/4
AMD Hardware Validated Boot (HVB)
0 or NC:Disable
1:Enable

EGPIO70 AT18 PM_PESLOT_AUX_RST# 21
EGPIO95 AW11 PEGX16_AUX_RST# 20
EGPIO96 AV12 EGPIO96_DRAM 57
EGPIO96 AW12 WIFI_AUX_RST# 23
EGPIO97 AU13 PM19_AUX_RST# 17
EGPIO98 AV13 M21_AUX_RST# 22
EGPIO99 AT14 LAN_AUX_RST# 28
EGPIO100

CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92 AT23 CLK_REQ0
CLK_REQ1_L/AGPIO115 AV24 CLK_REQ1_M.2 CLK_REQ1_M.2 22
CLK_REQ2_L/AGPIO116 AT24 CLK_REQ2
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/AGPIO131 AL23 PM19_CLK_REQ_L PM19_CLK_REQ_L 17
CLK_REQG_L/OSCIN/AGPIO132 AR22 CLK_REQG CLK_REQG 20
M2_1
RROM19
X16

USB_OC0_L/AGPIO16 AL1 APU_OC0 APU_OC0 37
USB_OC1_L/TDI/AGPIO17 AM1 LAN_WAKE#
USB_OC2_L/TCK/AGPIO18 AR1
USB_OC3_L/TDO/AGPIO24 AP1
3VSB
APU_OC0 R94 200K/4

VDDCR_CPU_SENSE F14 VDDCR_CPU_SENSE+ 25,41
VDDCR_SOC_SENSE E15 VDDCR_SOC_SENSE+ 41
VDDIO_MEM_S3_SENSE G14
VSS_SENSE_A F15 CP7 CP6 X_COPPER X_COPPER VDDIO_MEM_S3_SENSE 49
VDDCR_CPU_SENSE- 41
VDDCR_SOC_SENSE- 41
VDDP_SENSE AL22 CPU_VDDP_SENSE CPU_VDDP_SENSE 47
VSS_SENSE_B AM23 TP23

VCC3
R159 560R/4 SATA_LED#
R158 10K/4 CLK_REQ1_M.2
R156 X_10K/4 CLK_REQ2
R155 10K/4 CLK_REQG
R555 10K/4 PM19_CLK_REQ_L
R150 X_10K/4 CLK_REQ0
R154 X_10K/4 CLK_REQ1_M.2
R157 X_10K/4 CLK_REQ2
R537 X_10K/4 PM19_CLK_REQ_L
R149 X_10K/4 CLK_REQG

Layout:Place x'tal within 1.5 inch of APU
APU_32K_X2
Y2 32.768KHZ12.5p
APU_32K_X1
R120 20M/6
C136 12p50N6
C135 12p50N6
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

AM4 CPU TYPE Circuit

3VSB R142 1K/4
CORETYPE1

ATX_5VSB
R271 47K/4
TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS
TYPE0_CPU_SEL 7,47,48
CPU_1P8_S5
R276 1K/4
CORETYPE0
R280 4.7K/4
CORETYPE0R
Q28 2N3904
CORETYPE0
0:BR/SR/PR/MTS
1:RV

IB=(CPU_1P8_S5-Vbe)/5.7k
(1.8-0.95)/5.7k=0.149mA

IC=(VCC5-Vce)/47k
(5-0.2)/47k=0.102mA

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	1	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	0

3VSB PWR_1P8_SW
R170 10K/4
R171 10K/4
AGPIO9
N-PM514BA
Q15
TPM_HOLD# 7

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Document Description 06 AM4 SVI / ACPI / GPIO
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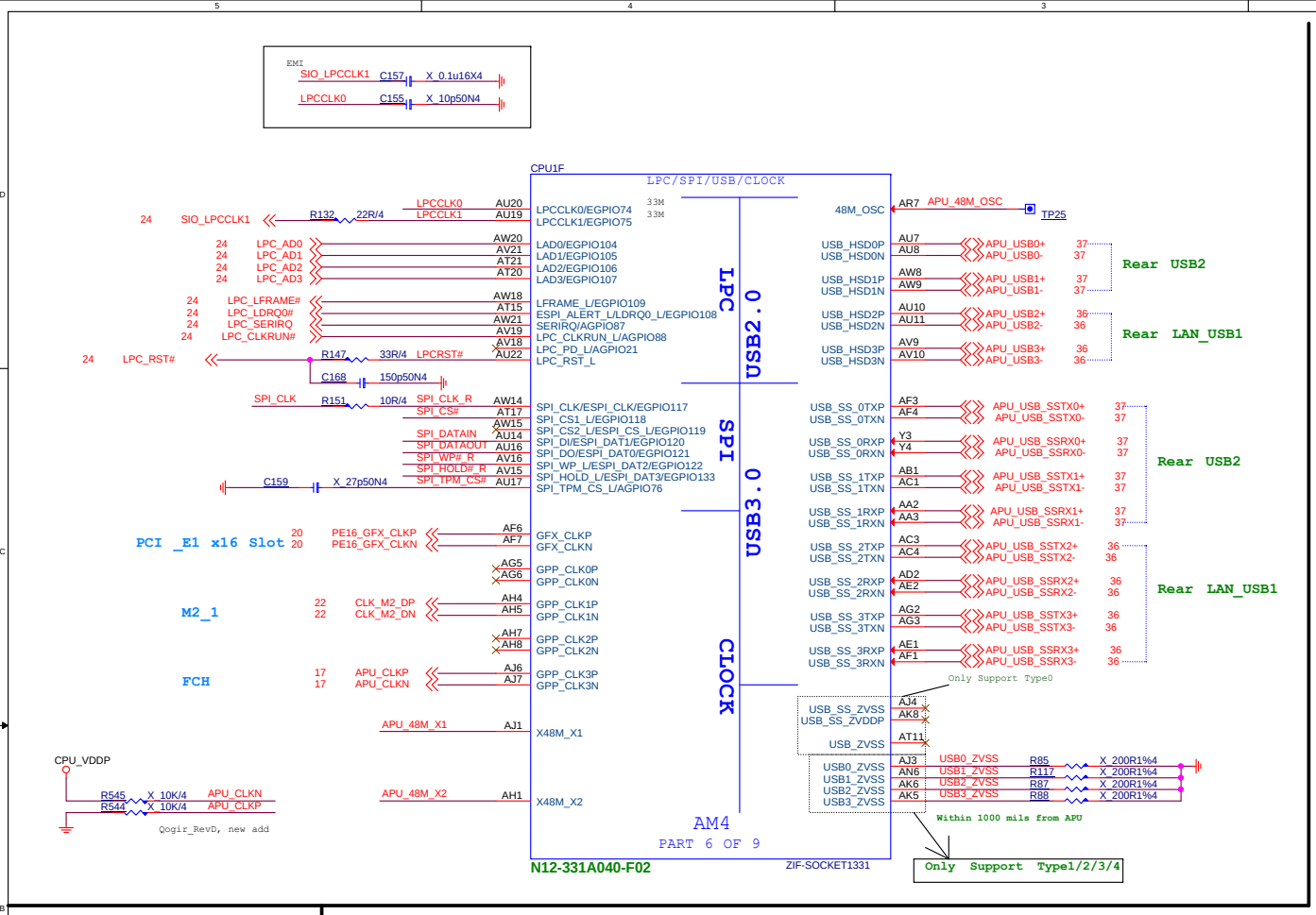
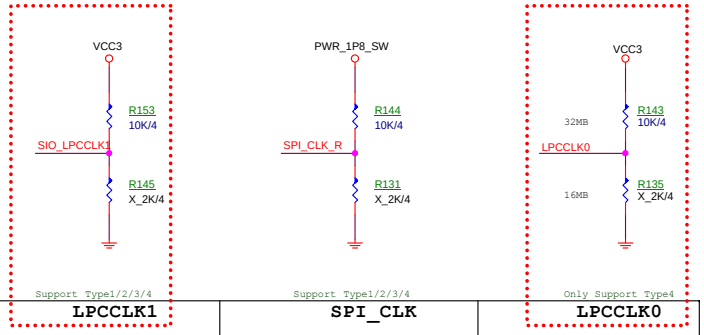
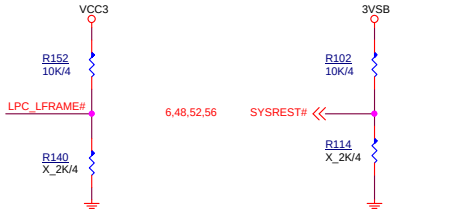


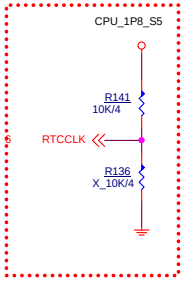
Strapping Options



	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image **(Default)**
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

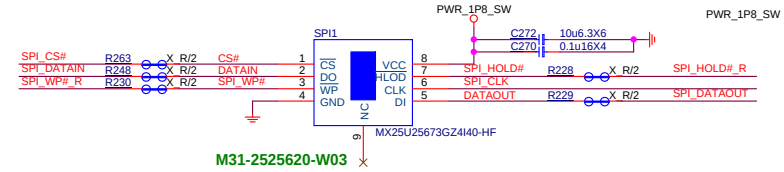


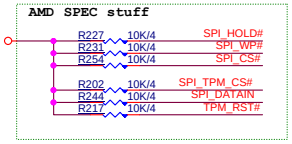
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	**(Default)** Traditional Reset logic	LPC ROM	short reset mode

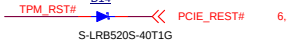


	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock **(Default)**
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

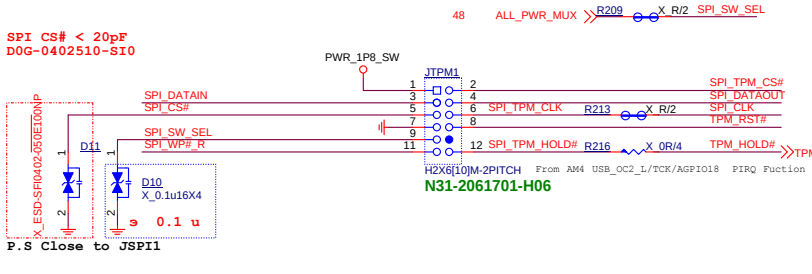
SPI ROM(1.8V)

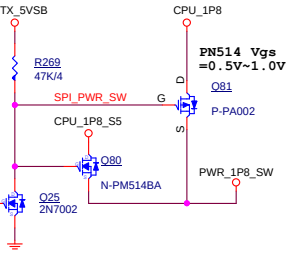


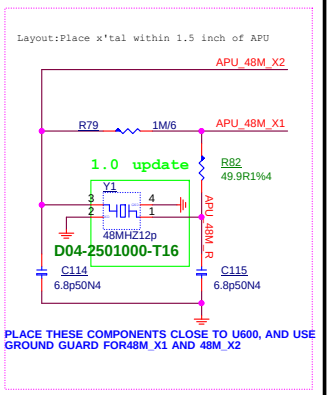




VDD_18 - Type 0, 2, and 4
VDD_18_S5 - Type 1 and 3







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MS-7D14	
Size: Custom	Document Description: 07 AM4 LPC / SPI /USB/CLK/STRAP — Rev: 21
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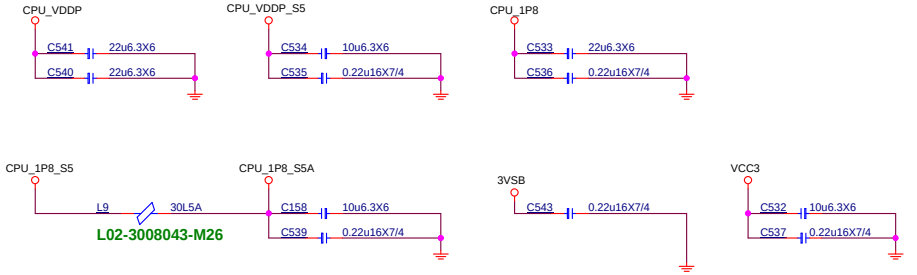
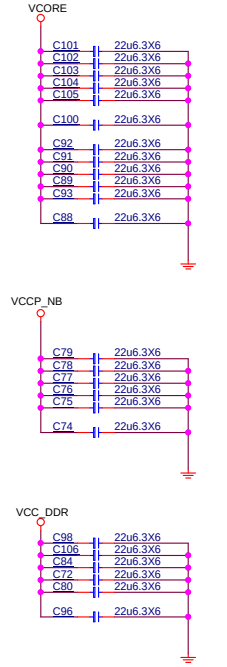
TOP and BOTTOM SIDE

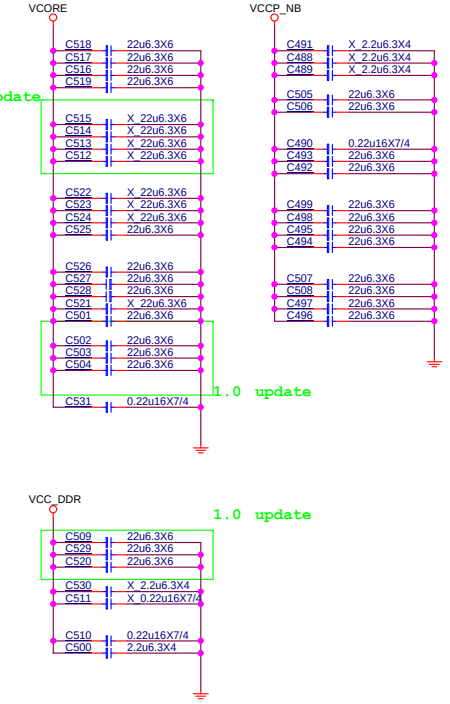


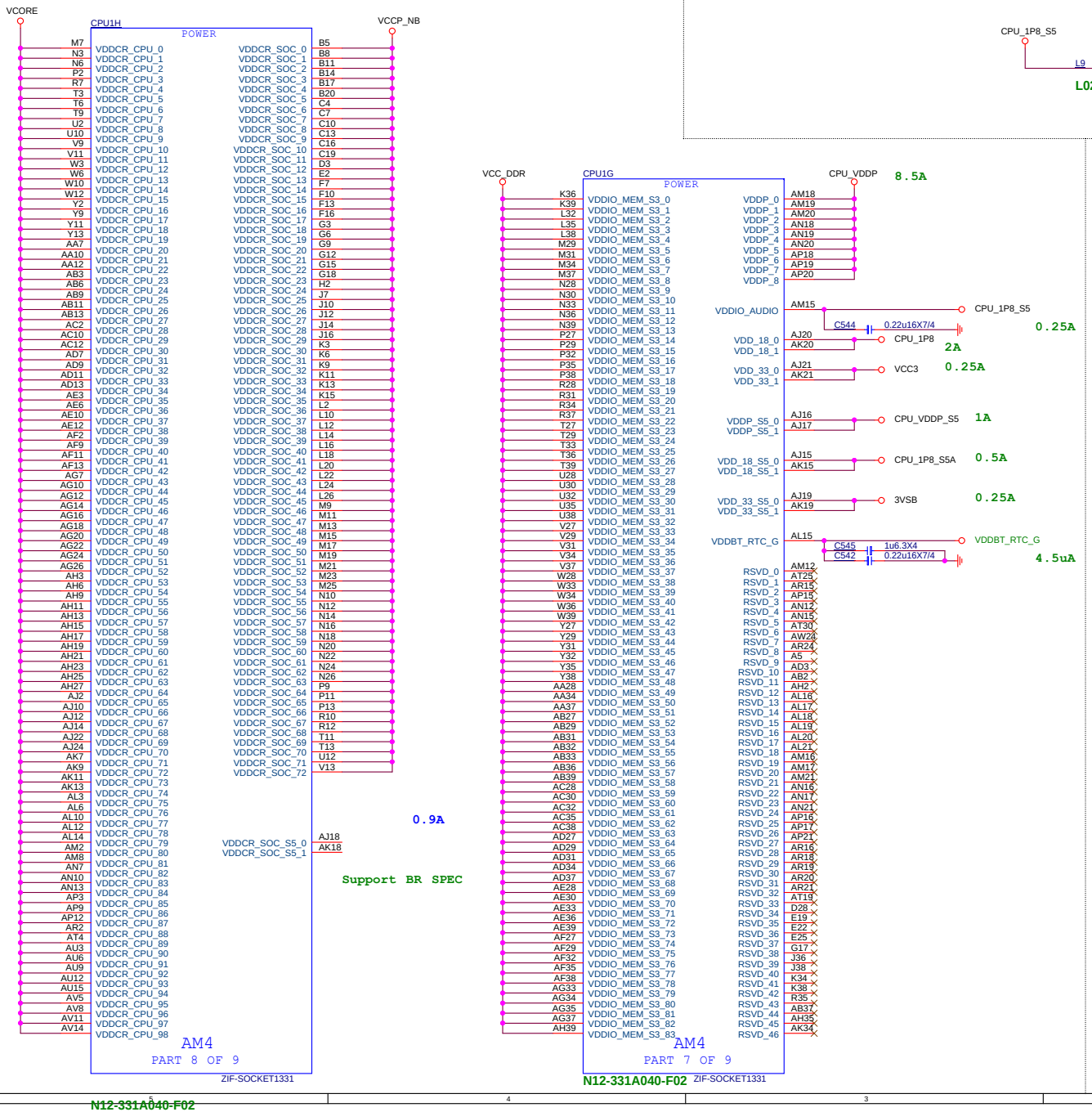
TOP CAVITY

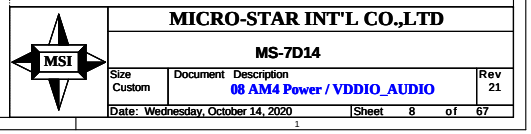


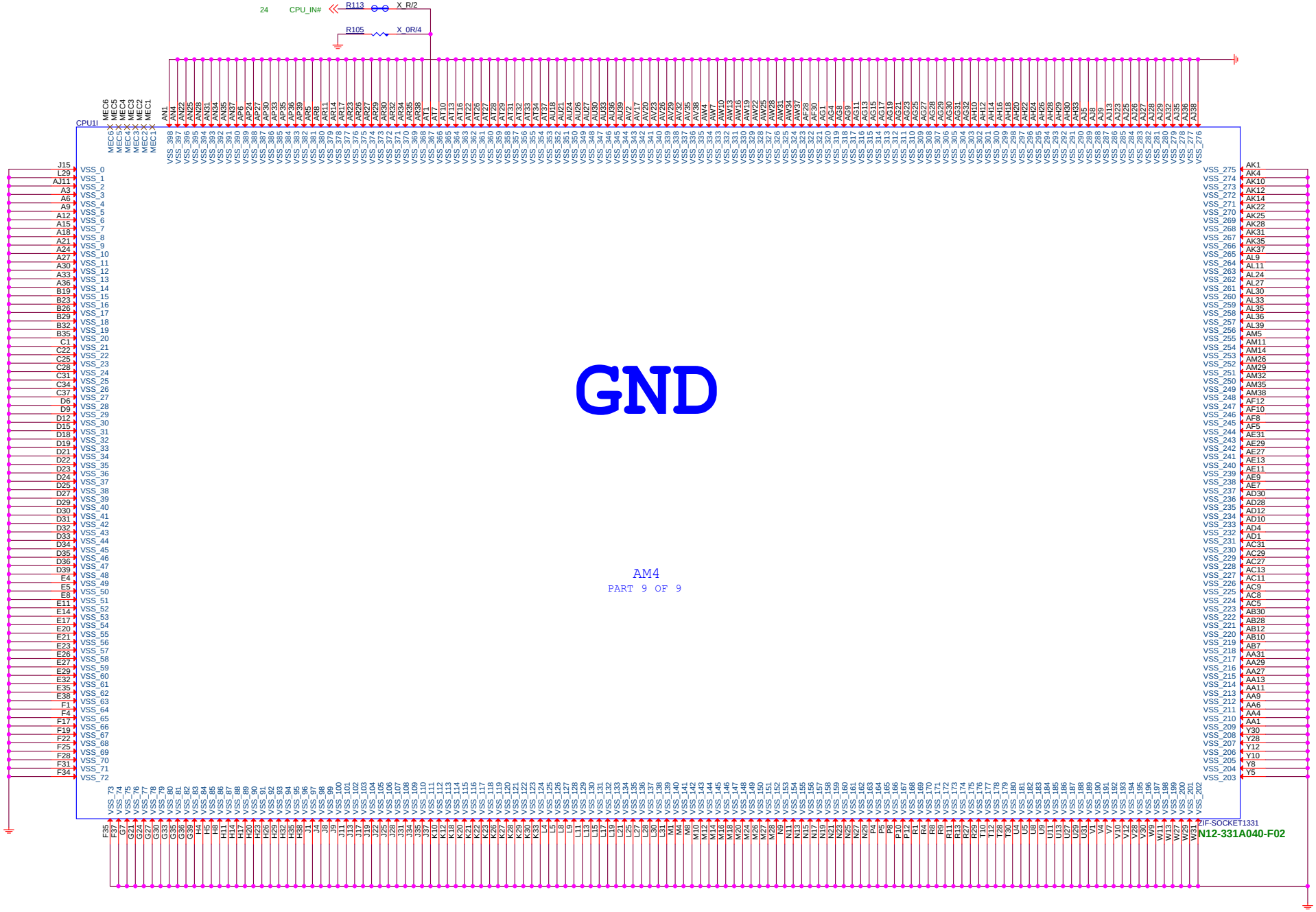
add for cross moat

BOTTOM CAVITY









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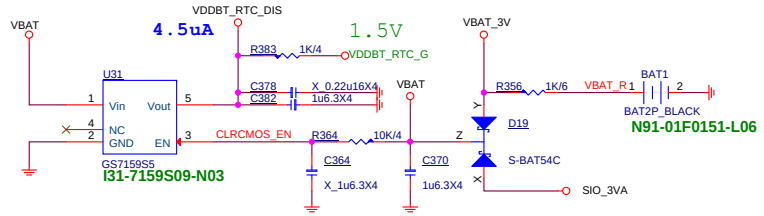
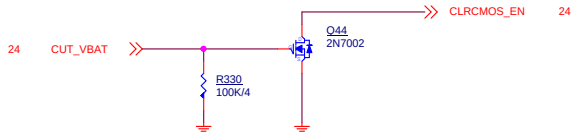
RTC & Clear CMOS Circuit

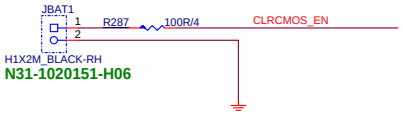
VDDBT_RTC_G	1.50	All	4.5uA	–	–





RTC Backup

Clear CMOS button



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SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

6,53 SCLK0 SCLK0 R174 X R/2 SMB_CLK_DIMM SMB_CLK_DIMM 12
6,53 SDATA0 SDATA0 R178 X R/2 SMB_DATA_DIMM SMB_DATA_DIMM 12

MICRO-STAR INT'L CO.,LTD

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Custom	11 DDR4 - DIMM CH-A	21

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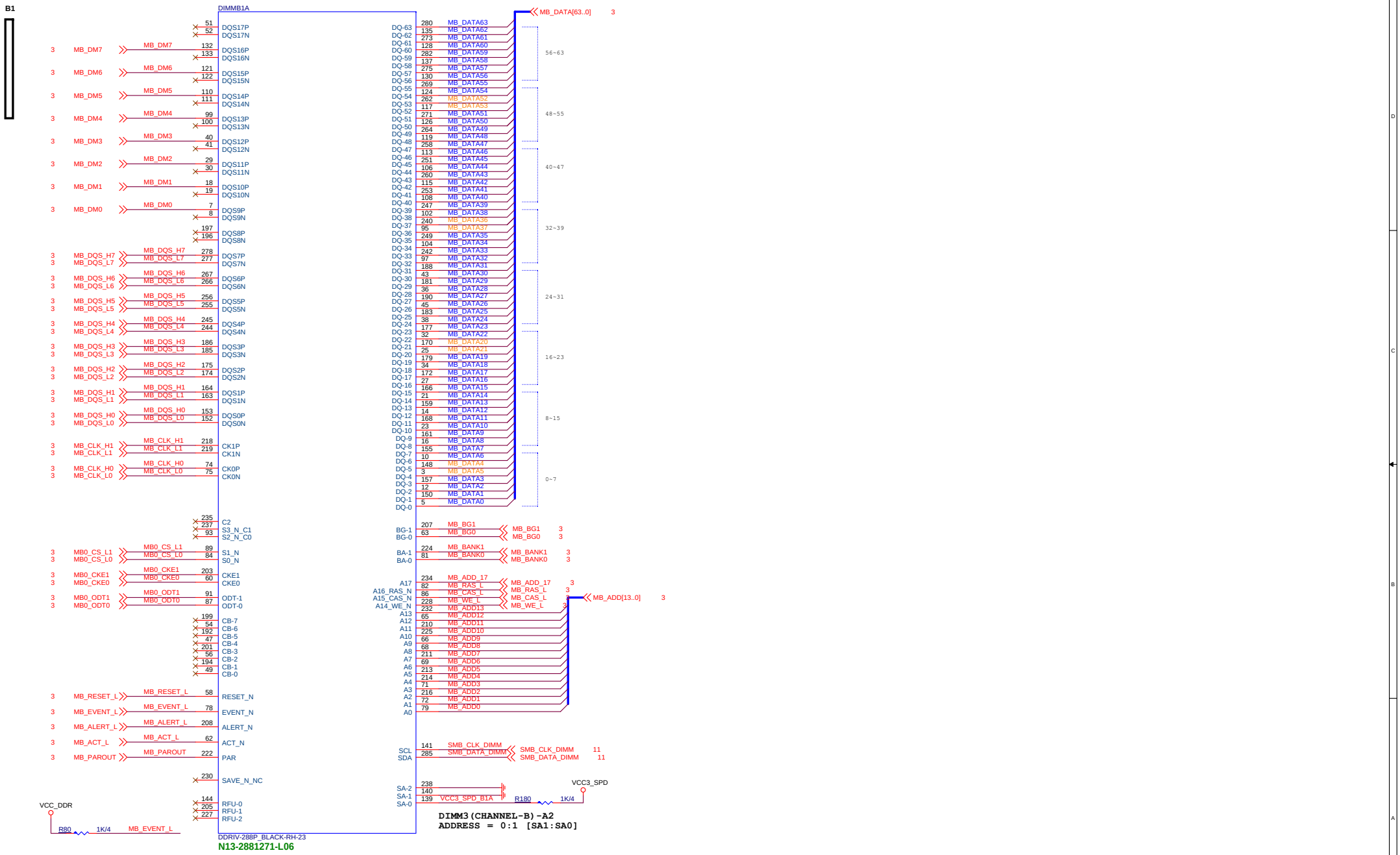
B1
DIMMB1A
MB_DATA[63..0]
MB_ADD[13..0]
MB_DM7
MB_DM6
MB_DM5
MB_DM4
MB_DM3
MB_DM2
MB_DM1
MB_DM0
MB_DQS_H7
MB_DQS_L7
MB_DQS_H6
MB_DQS_L6
MB_DQS_H5
MB_DQS_L5
MB_DQS_H4
MB_DQS_L4
MB_DQS_H3
MB_DQS_L3
MB_DQS_H2
MB_DQS_L2
MB_DQS_H1
MB_DQS_L1
MB_DQS_H0
MB_DQS_L0
MB_CLK_H1
MB_CLK_L1
MB_CLK_H0
MB_CLK_L0
MB0_CS_L1
MB0_CS_L0
MB0_CKE1
MB0_CKE0
MB0_ODT1
MB0_ODT0
MB_RESET_L
MB_EVENT_L
MB_ALERT_L
MB_ACT_L
MB_PAROUT
MB_BG1
MB_BG0
MB_BANK1
MB_BANK0
MB_ADD_17
MB_RAS_L
MB_CAS_L
MB_WE_L
SMB_CLK_DIMM
SMB_DATA_DIMM
VCC3_SPD
VCC_DDR
R80
1K/4
R180
DDRIV-288P_BLACK-RH-23
N13-2881271-L06
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
MICRO-STAR INT'L CO.,LTD
MS-7D14
Size Custom
Document Description 12 DDR4 - DIMM CH-B
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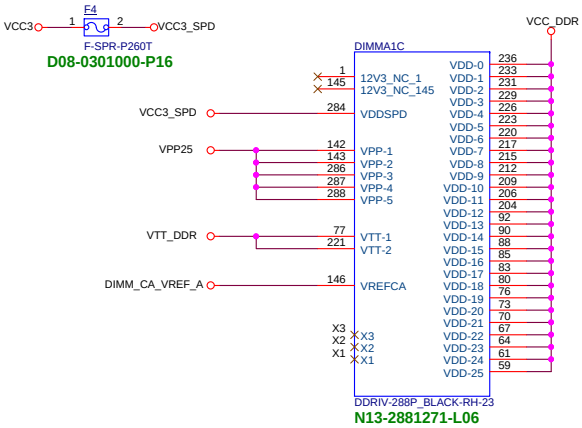
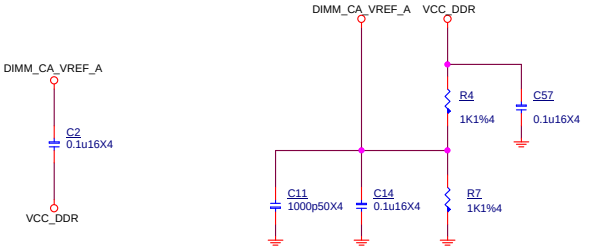
avl:D08-0301100-B07

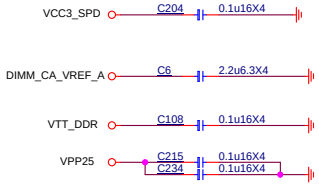


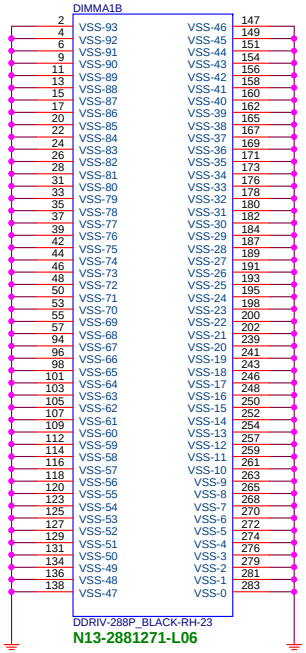
DIMM SLOT PN BY SPEC

DDR VREF

(place resistors close to DIMMs)







MICRO-STAR INT'L CO.,LTD

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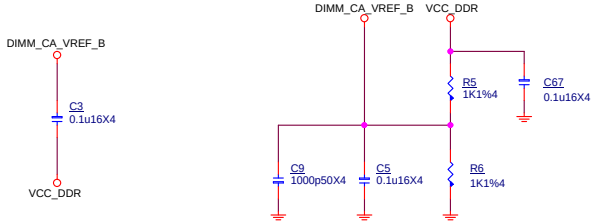
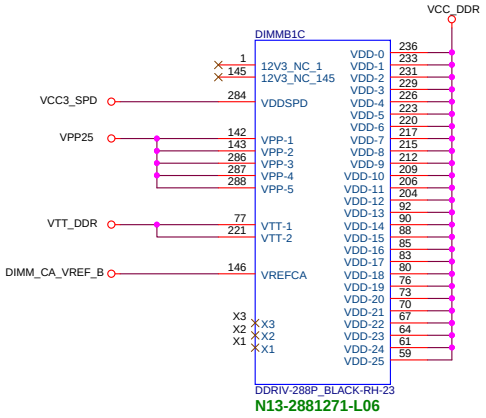
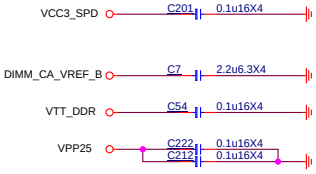
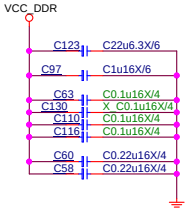
DDR VREF

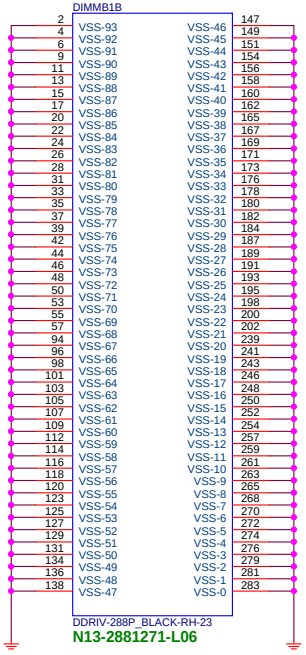
(place resistors close to DIMMs)











MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7D14	
Size: Custom	Document Description: 14 DDR4 - POWER/GND-2	Rev: 21
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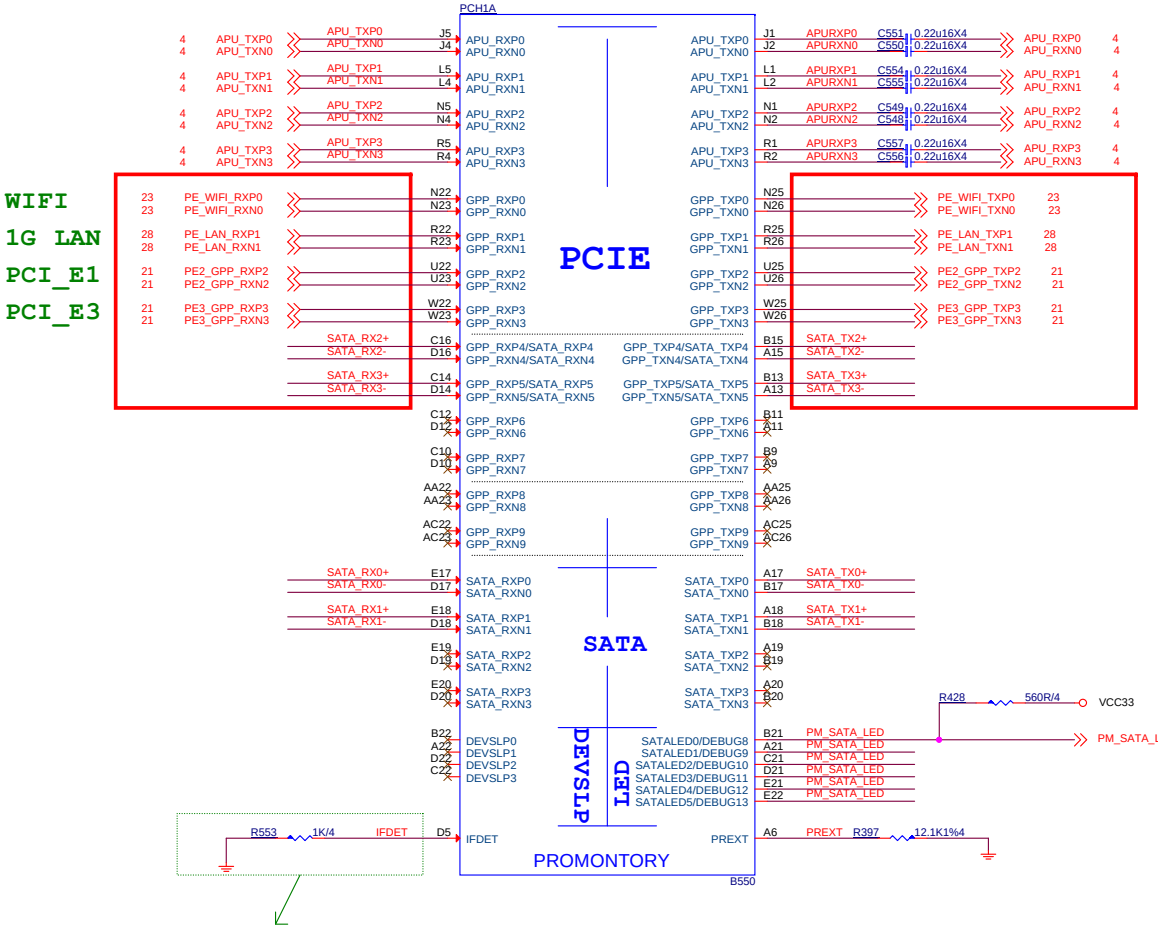
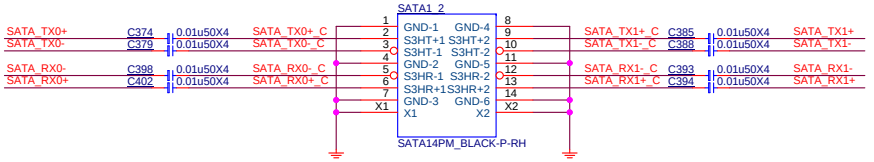
SATA Connector

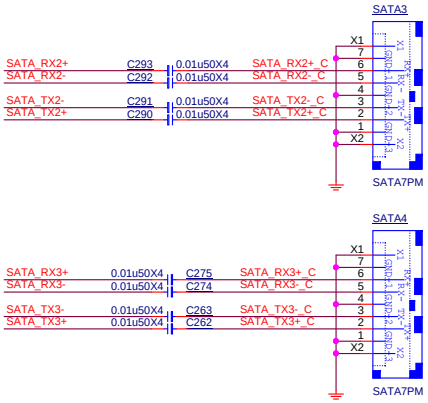


PCIe/SATA combo mode select (GPP[5:4]/SATA[5:4])
0:SATA Mode
1:PCIE Mode

SATA1_2



AVL:N5N-14M0201-L06



MICRO-STAR INT'L CO.,LTD		
MS-7D14		
Size: Custom	Document Description: 15 PROM19 - PCIE/SATA	Rev: 21
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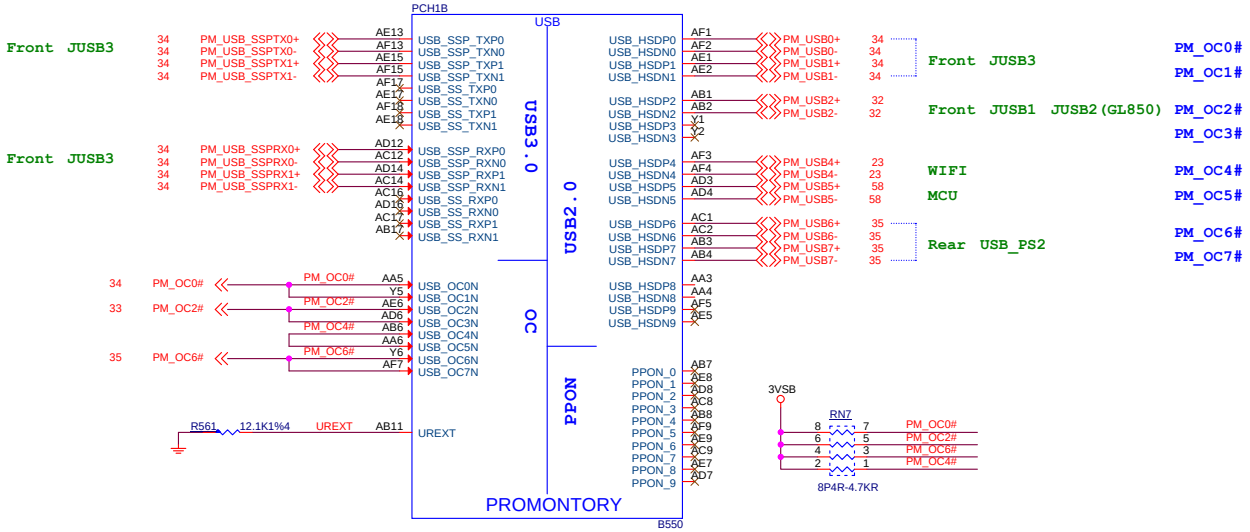

USB mapping

USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
USB_HSDP/N[4] + USB_OC4N
USB_HSDP/N[5] + USB_OC5N
USB_HSDP/N[6] + USB_OC6N
USB_HSDP/N[7] + USB_OC7N
USB_HSDP/N[8] + USB_OC7N
USB_HSDP/N[9] + USB_OC7N

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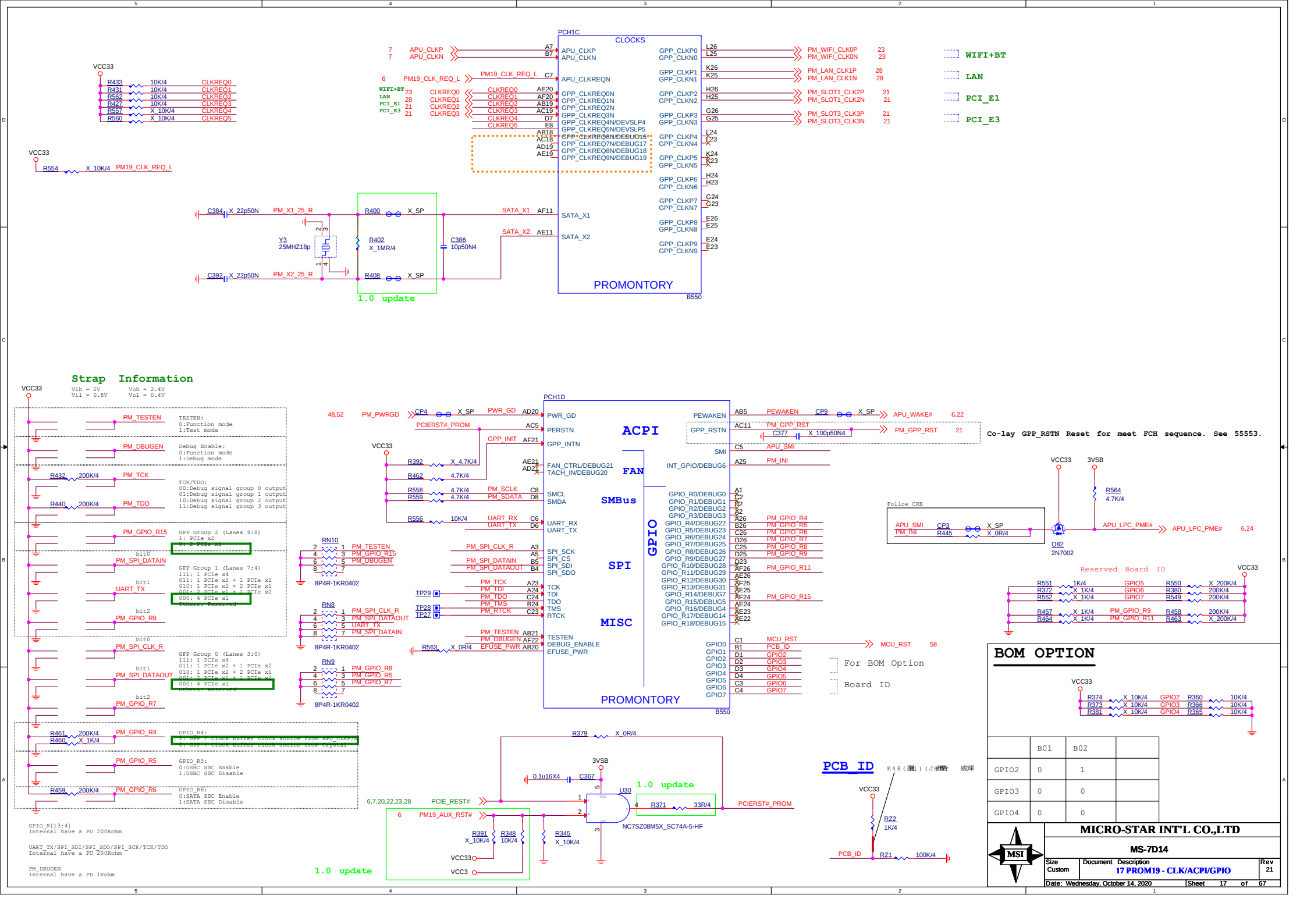
PCH1C
CLOCKS
PROMONTORY
B550
WIFI+BT
LAN
PCI_E1
PCI_E3
1.0 update
Strap Information
Vih = 2V
Vil = 0.8V
Voh = 2.4V
Vol = 0.4V
PCH1D
ACPI
FAN
SMBus
SPI
MISC
GPIO
Co-lay GPP_RSTN Reset for meet FCH sequence. See 55553.
Follow CRB
Reserved Board ID
For BOM Option
Board ID
BOM OPTION
PCB_ID
MICRO-STAR INT'L CO.,LTD
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17 PROM19 - CLK/ACPI/GPIO
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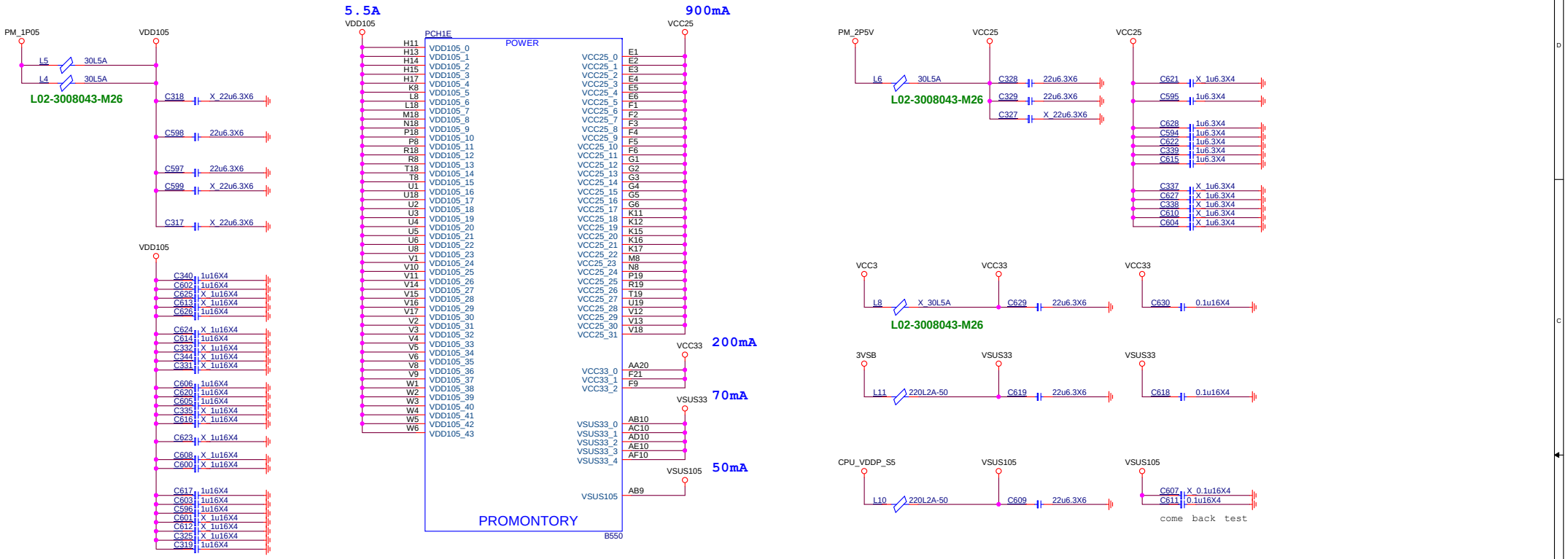

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: 18 PROM19 - Power	Rev: 21
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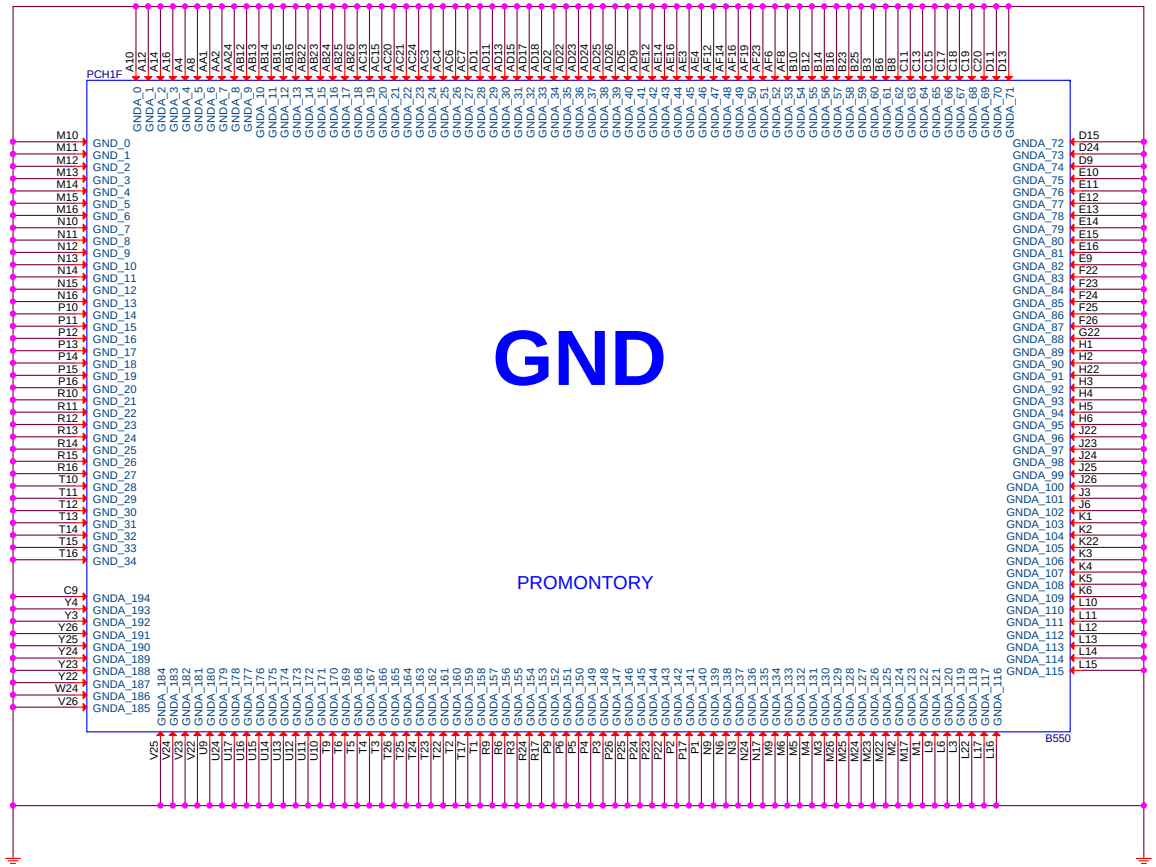

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Size: Custom	Document Description: 19 PROM19 - GND
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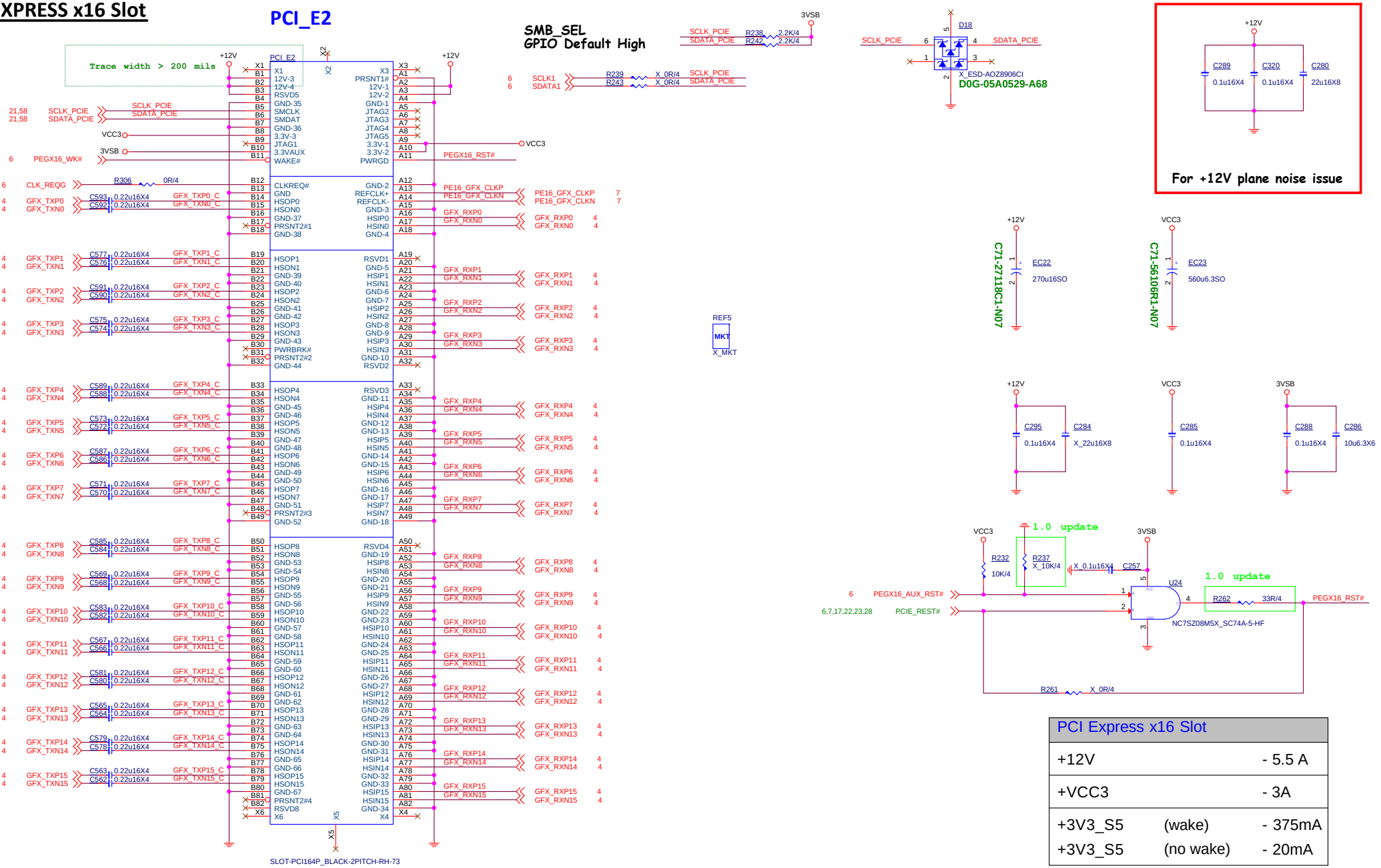
PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Size: Custom	Document Description: 20 PCI_E1 (X16)
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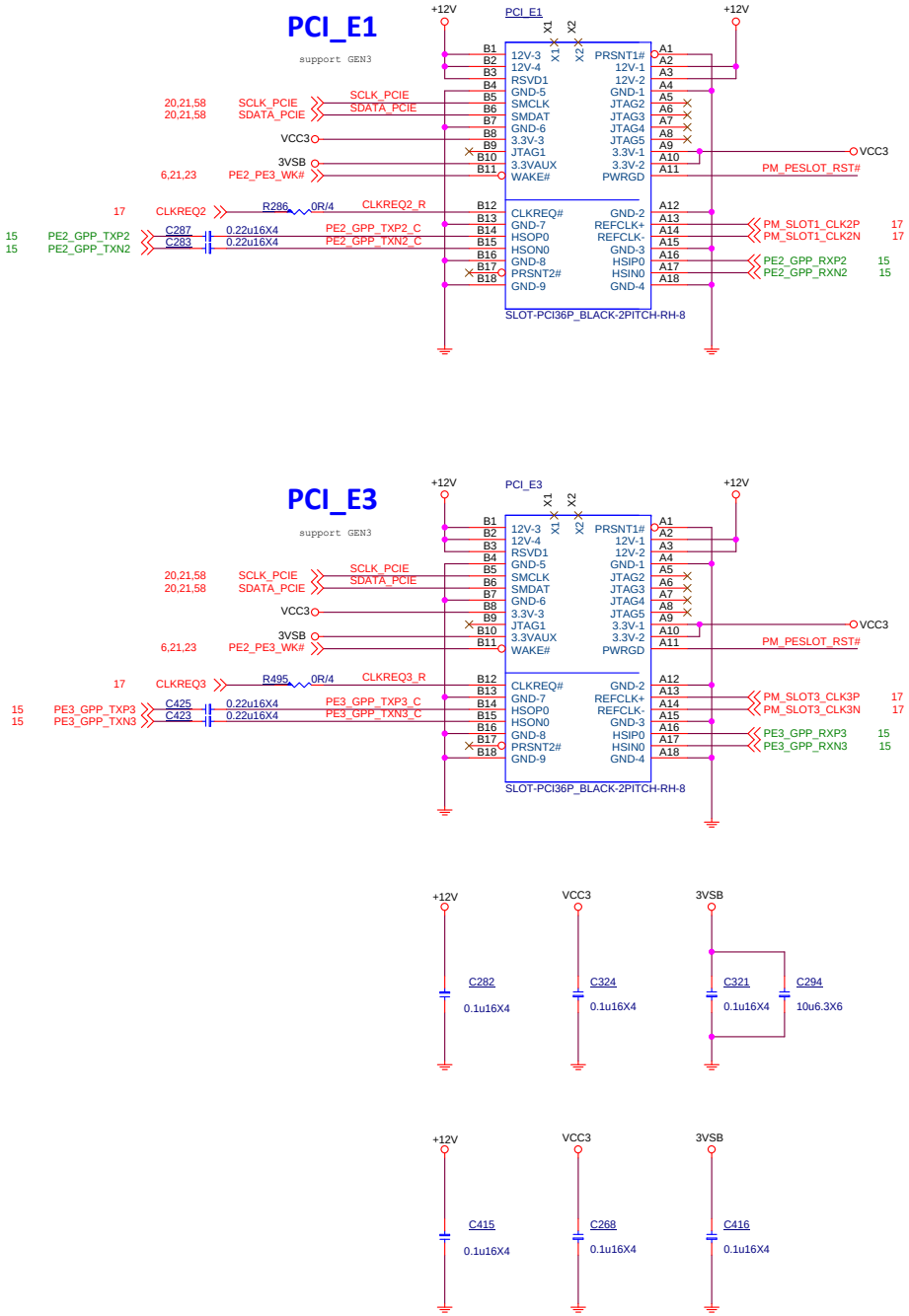
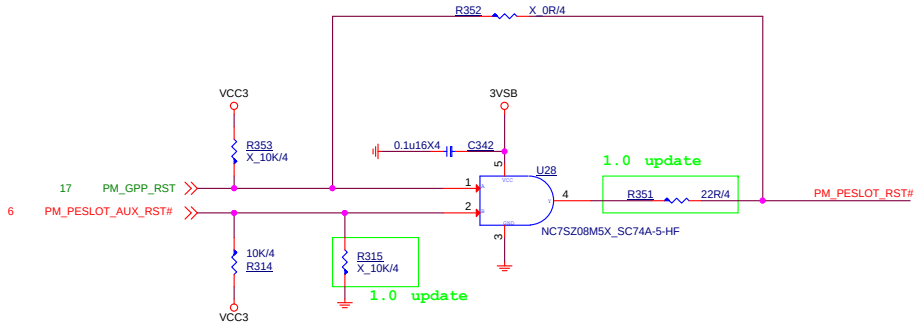
PCI EXPRESS X1 SLOT



12V - 0.5A

VCC3 - 3A

3VSBV - 375mA



PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD

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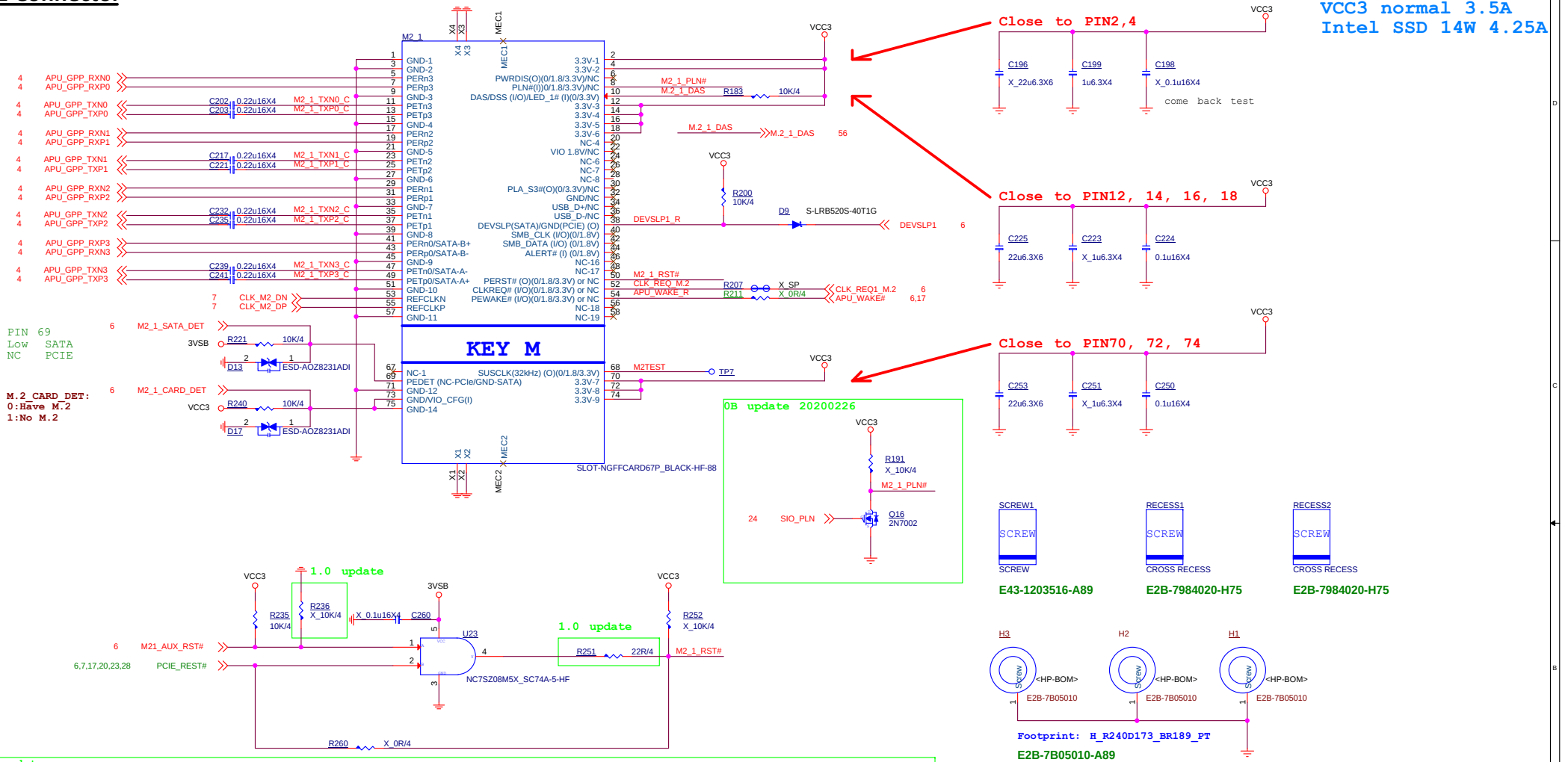
M.2 1 Connector

M2 插槽 综 蔼 璶 0.9mm 築ン

VCC3 peak 7A
VCC3 normal 3.5A
Intel SSD 14W 4.25A



Close to PIN2,4

Close to PIN12, 14, 16, 18

Close to PIN70, 72, 74

0B update 20200226

1.0 update

1.0 update

MICRO-STAR INT'L CO.,LTD

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Custom	22 M2_1 PCIE / SATA	21

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EMI

NEAR CONNECTOR

16 PM_USB4+ — PM_USB4+ — U17 (ESD-AOZ8906CI) — PM_USB4+ 16

16 PM_USB4- — PM_USB4- — U17 (ESD-AOZ8906CI) — PM_USB4- 16

3VSB — C191 X_0.1u16X4

ATX_5VSB — R546 47K/4 — Q78 2N7002D — D2 BT_DISABLE_L#

3VSB — R538 47K/4 — G1 WIFI_BTDIS# — 24 WIFI_BTDIS#

ATX_5VSB — R547 47K/4 — Q79 2N7002D — D2 WIFI_DISABLE_L#

WIFI_BTDIS# — G1

COVER1 — VR Cover — X1 — X2 — X_E21-4467011-C22

E21-4467011-C22

WF_SCREW1 SCREW SCREW

WF_SCREW2 SCREW SCREW

E43-1204046-P65 E43-1204046-P65

Wireless1 — Intel 3168NGW — MS-4467 Wireless

604-4467-040

780mA

3VSB — come back test

C189 X_1u6.3X4

C184 10u6.3X6

C188 0.01u50X4

M2_WIFI1 MEC2

1	GND-1	3.3V-1	2
PM_USB4+ 3	USB_D+	3.3V-2	4
PM_USB4- 5	USB_D-	LED1#	6
7	GND-11	PCM_CLK / I2S SCK	8
9	SDIO CLK	PCM_SYNC / I2S WS	10
11	SDIO CMD	PCM_IN / I2S SD_IN	12
13	SDIO DATA0	PCM_OUT / I2S SD_OUT	14
15	SDIO DATA1	LED2#	16
17	SDIO DATA2	GND-2	18
19	SDIO DATA3	UART WAKE#	20
21	SDIO WAKE#	UART RXD	22
23	SDIO RESET#		

KEY E

33	GND-10	UART TXD	32
15 PE_WIFI_TXP0 — 0.22u16X4 C207 — PE_WIFI_TXP0_C	35 PETp0	UART CTS	34
15 PE_WIFI_TXN0 — 0.22u16X4 C216 — PE_WIFI_TXN0_C	37 PETn0	UART RTS	36
39	GND-9	VENDOR DEFINED-1	38
15 PE_WIFI_RXP0	41 PERp0	VENDOR DEFINED-2	40
15 PE_WIFI_RXN0	43 PERn0	VENDOR DEFINED-3	42
45	GND-8	COEX3	44
17 PM_WIFI_CLK0P	47 REFCLKP0	COEX2	46
17 PM_WIFI_CLK0N	49 REFCLKN0	COEX1	48
51	GND-7	SUSCLK	50 WIFI_BT_RTCCLK_R — R169 0R/4 — WIFI_BT_RTCCLK 6
17 CLKREQ0 — R185 X_R/2 — CLKREQ0_R	53 CLKREQ0#	PERST0#	52 WIFI_RST#
6,21 PE2_PE3_WK# — D8 S-LRB520S-40T1G	55 PEWAKE0#	W_DISABLE2#	54 BT_DISABLE_L# — R168 3.3KR/4 — 3VSB
24,28 SIO_LAN_WAKE# — D7 S-LRB520S-40T1G — WIFI_LAN_WAKE#		W_DISABLE1#	56 WIFI_DISABLE_L# — R167 3.3KR/4
57	GND-6	I2C DATA	58
3VSB — R184 10K/4 — WIFI_LAN_WAKE#	59 RESERVED / PETp1	I2C CLK	60
	61 RESERVED / PETn1	ALERT#	62
63	GND-5	RESERVED	64
	65 RESERVED / PERp1	UIM_SWP / PERST1#	66
	67 RESERVED / PERn1	UIM_POWER_SNK / CLKREQ1#	68
69	GND-4	UIM_POWER_SRC/GPIO1 / PEWAKE1#	70
	71 RESERVED / REFCLKP1	3.3V-3	72 — 3VSB
	73 RESERVED / REFCLKN1	3.3V-4	74 — C182 0.01u50X4 — C187 X_1u6.3X4 — C190 10u6.3X6
75	GND-3		

N15-0670610-L06 MEC1 SLOT-NGFFCARD67P_BLACK-HF-46

1.0 update

VCC3 — R161 10K/4 — R160 X_10K/4 — 0.1u16X4 C177 — 3VSB

1.0 update

6 WIFI_AUX_RST# — U15 — R166 33R/4 — WIFI_RST#

6,7,17,20,22,28 PCIE_REST# — U15

NC7SZ08M5X_SC74A-5-HF

R165 X_0R/4

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	24 M2_WIFI1 (KEY_E)	21

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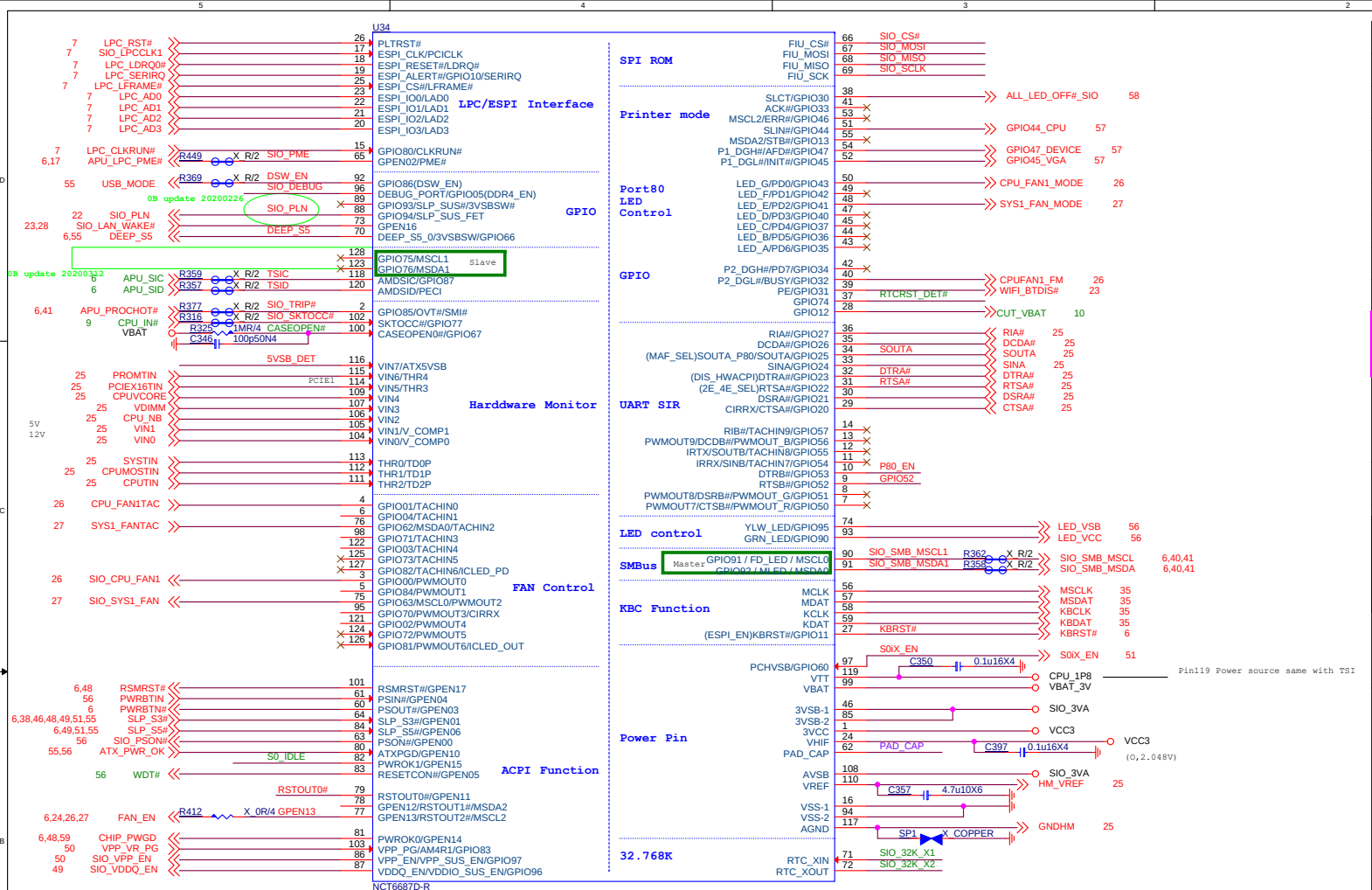
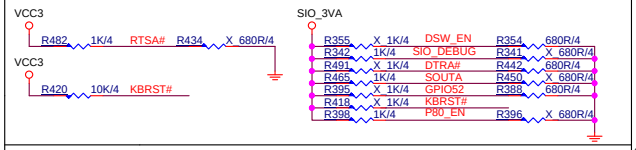


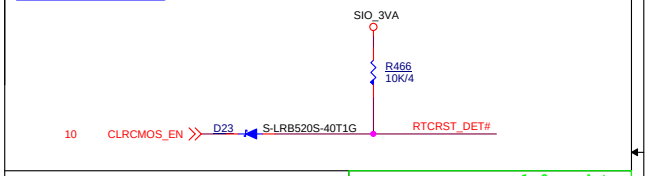
POWER ON STRAPPING PIN FOR NCT6687D-R

PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
10	P80_EN	GPIO46	Port80 LED	GPIO	3VA

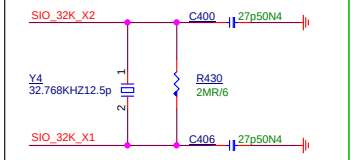
PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA



RTCRST DET



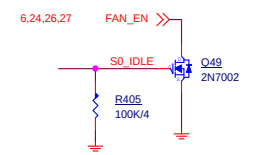
RTC 32K

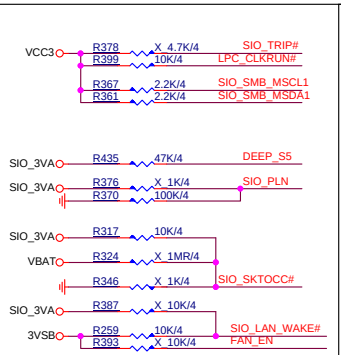


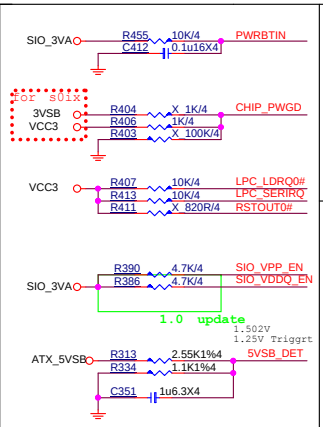
S0 IDLE

1.0 update

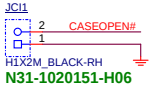
Closed FAN , by S0i3.



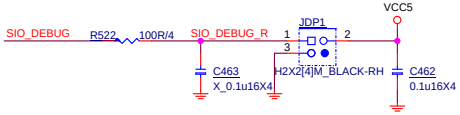




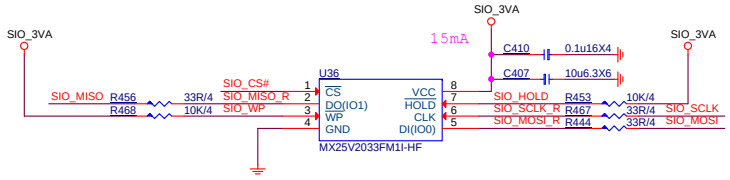
JCI1



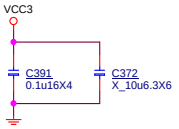
DEBUG PORT



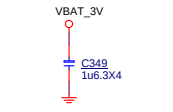
SPI ROM



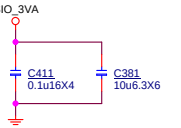
Closed PIN1,24



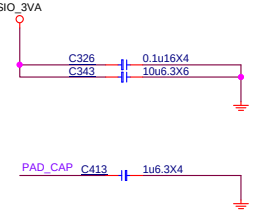
Closed PIN99



Closed PIN46,85



3V Analog Power



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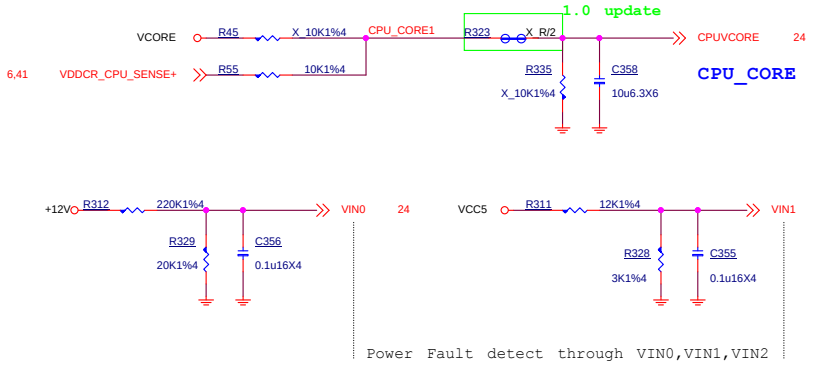
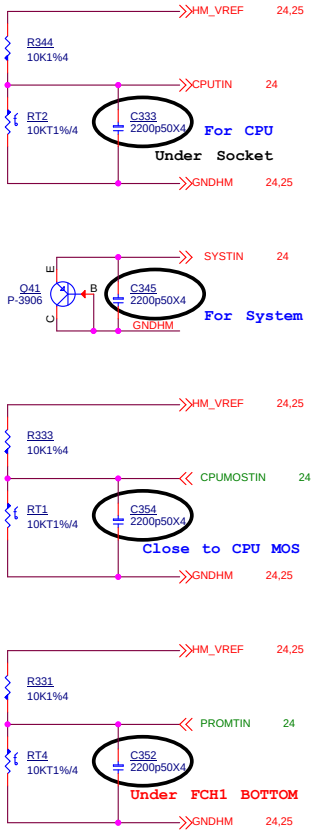
HW Monitor - Voltage

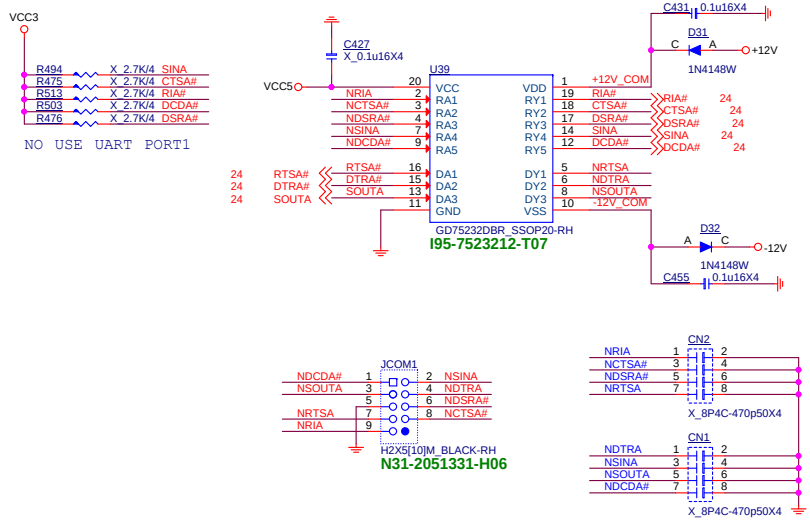
SIO HM Voltage over 2.048V will not detect



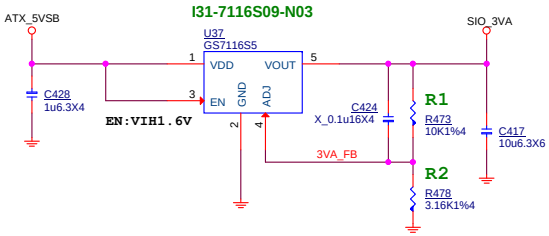
TEMP SENSOR



COM PORT



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MSI	MICRO-STAR INT'L CO.,LTD	
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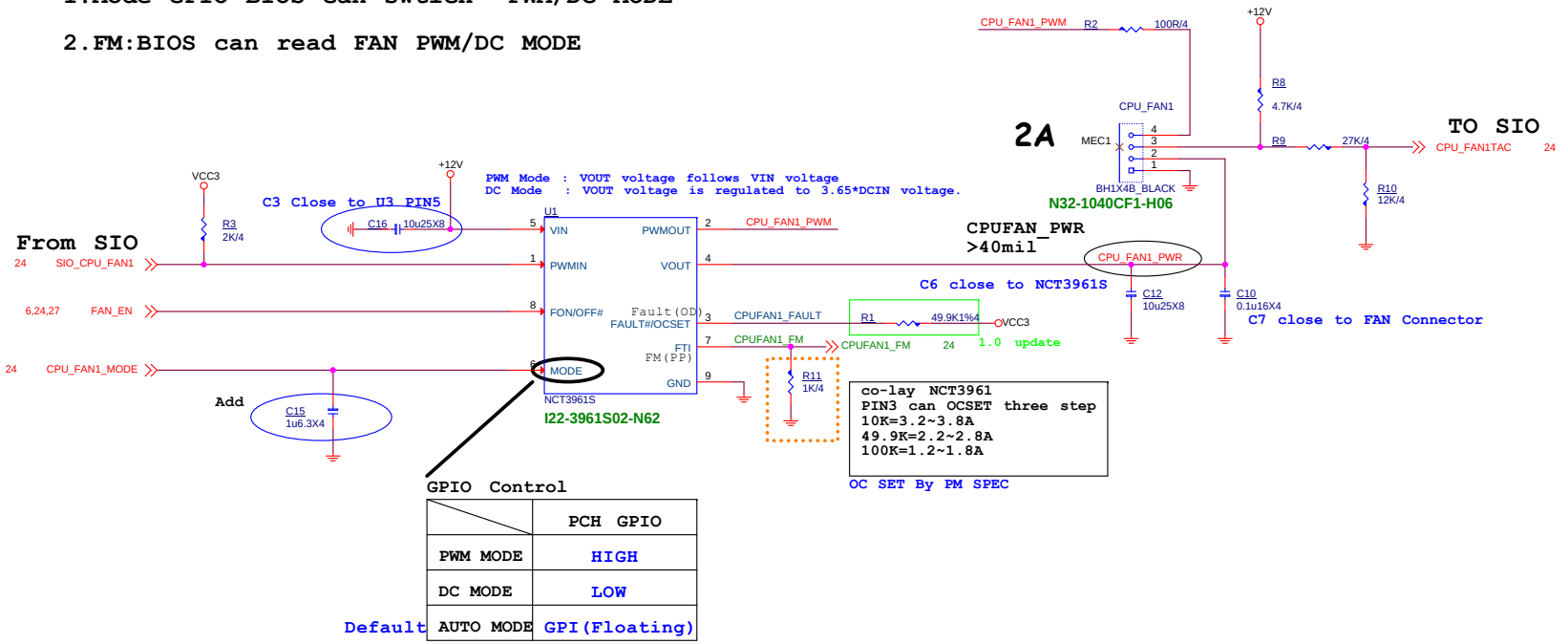
CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A

OC SET By PM SPEC

GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: 27 FAN TYPE-N CPUFAN1 | Rev: 21

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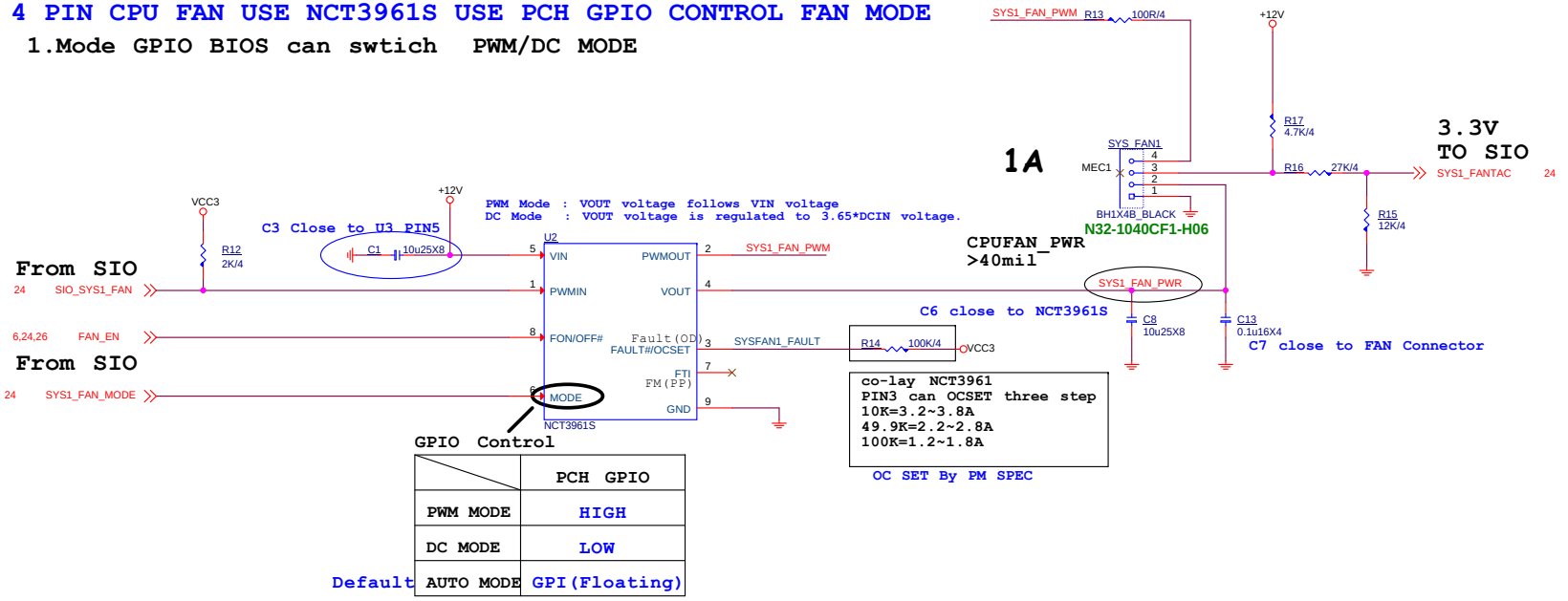
SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

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Size: Custom	Document Description: 29 FAN TYPE-M SYSFAN1 / 2 — Rev: 21
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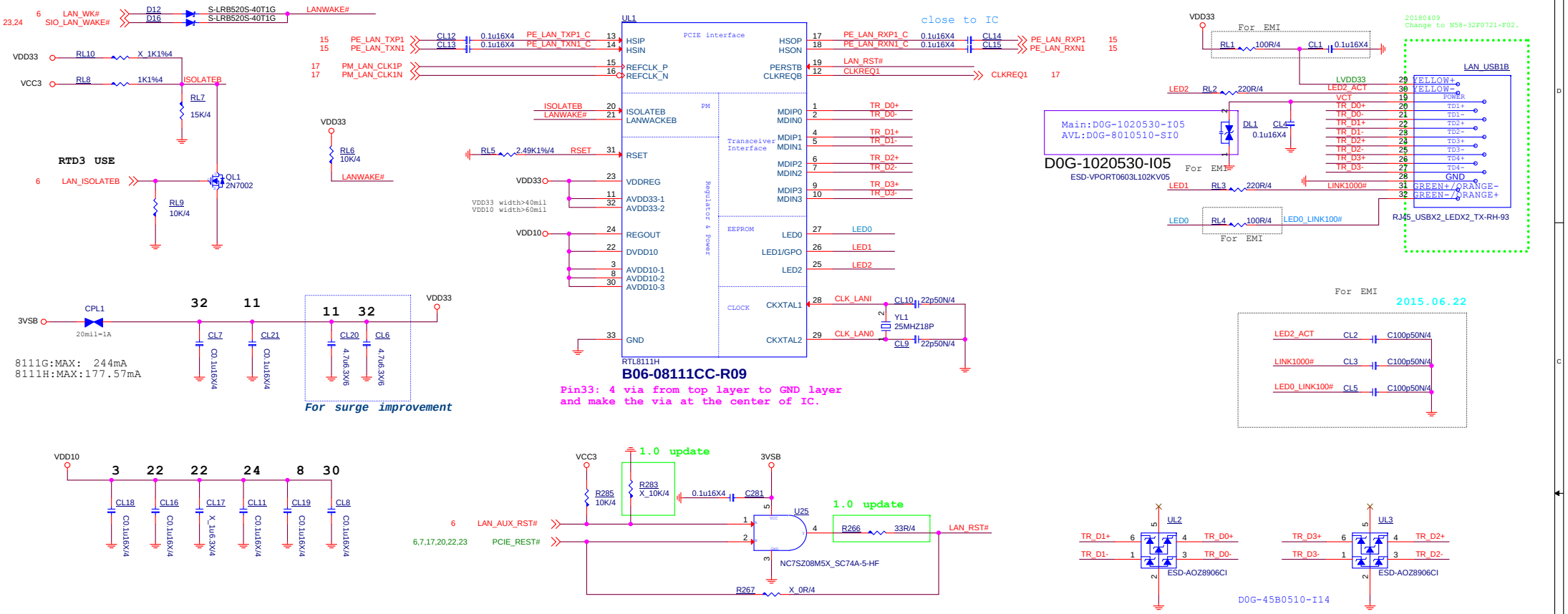
RTL8111G/RTL8111H Giga LAN



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MS-7D14	
Size: Custom	Document Description: 31 LAN - RTL8111EPV co-lay HN
Rev: 21	
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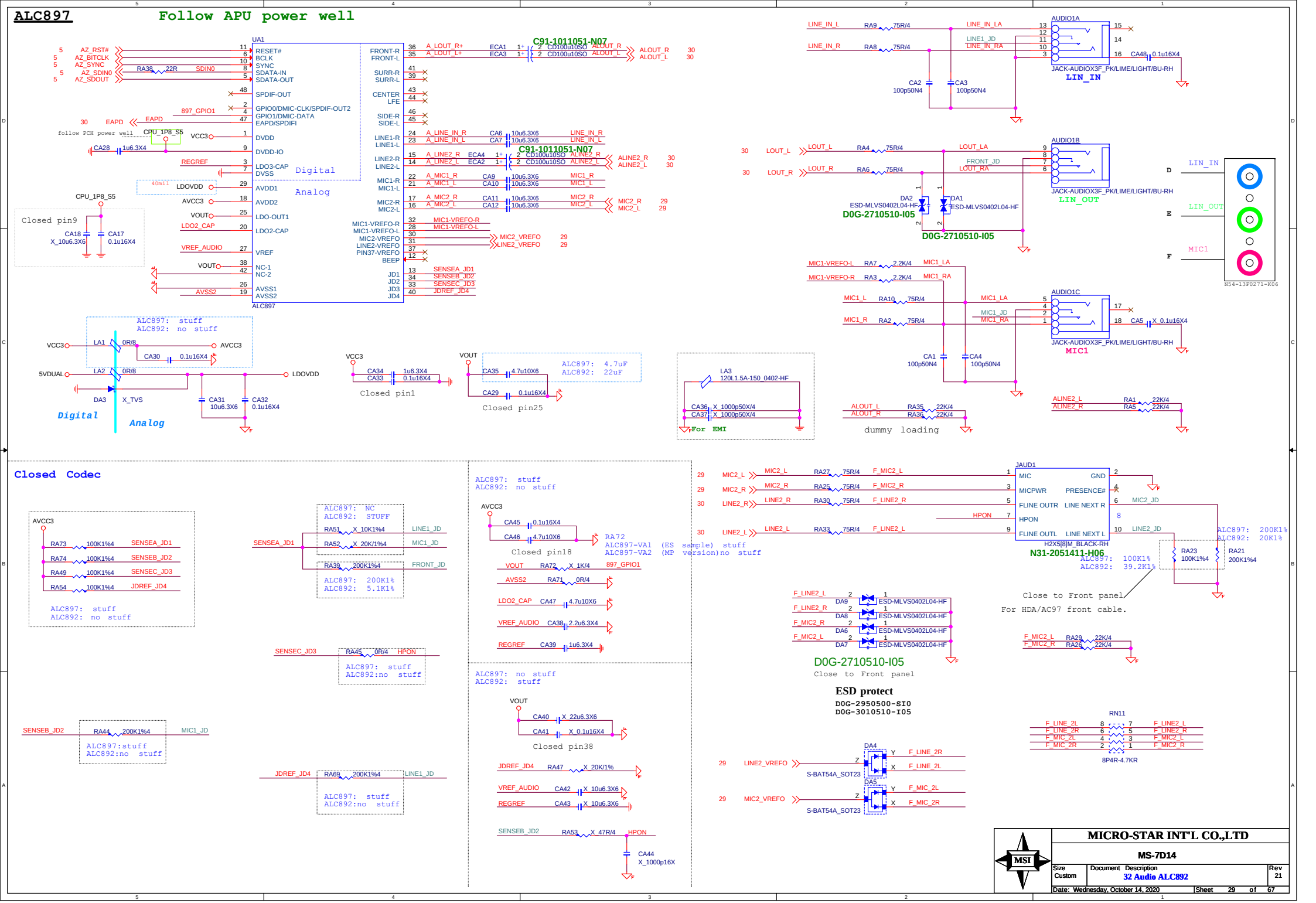
ALC897
Follow APU power well
UA1
ALC897
Digital
Analog
C91-1011051-N07
AUDIO1A
JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH
LIN_IN
AUDIO1B
LIN_OUT
D0G-2710510-I05
AUDIO1C
MIC1
N54-13F0271-K06
Closed pin9
Closed pin1
Closed pin25
ALC897: stuff
ALC892: no stuff
ALC897: 4.7uF
ALC892: 22uF
For EMI
dummy loading
Closed Codec
ALC897: NC
ALC892: STUFF
ALC897: 200K1%
ALC892: 5.1K1%
Closed pin18
RA72
ALC897-VA1 (ES sample) stuff
ALC897-VA2 (MP version) no stuff
JAUD1
H2X5[8]M_BLACK-RH
N31-2051411-H06
ALC897: 100K1%
ALC892: 39.2K1%
ALC897: 200K1%
ALC892: 20K1%
Close to Front panel
For HDA/AC97 front cable.
D0G-2710510-I05
Close to Front panel
ESD protect
D0G-2950500-SI0
D0G-3010510-I05
RN11
8P4R-4.7KR
Closed pin38
S-BAT54A_SOT23
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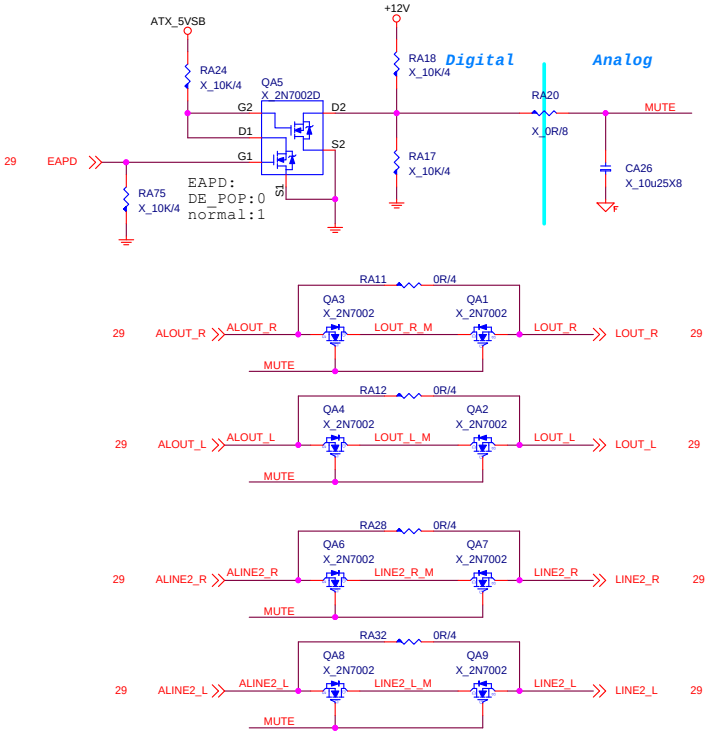
Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)



MICRO-STAR INT'L CO.,LTD			
MS-7D14			
Size: Custom	Document Description: 33 Audio DePoP		Rev: 21
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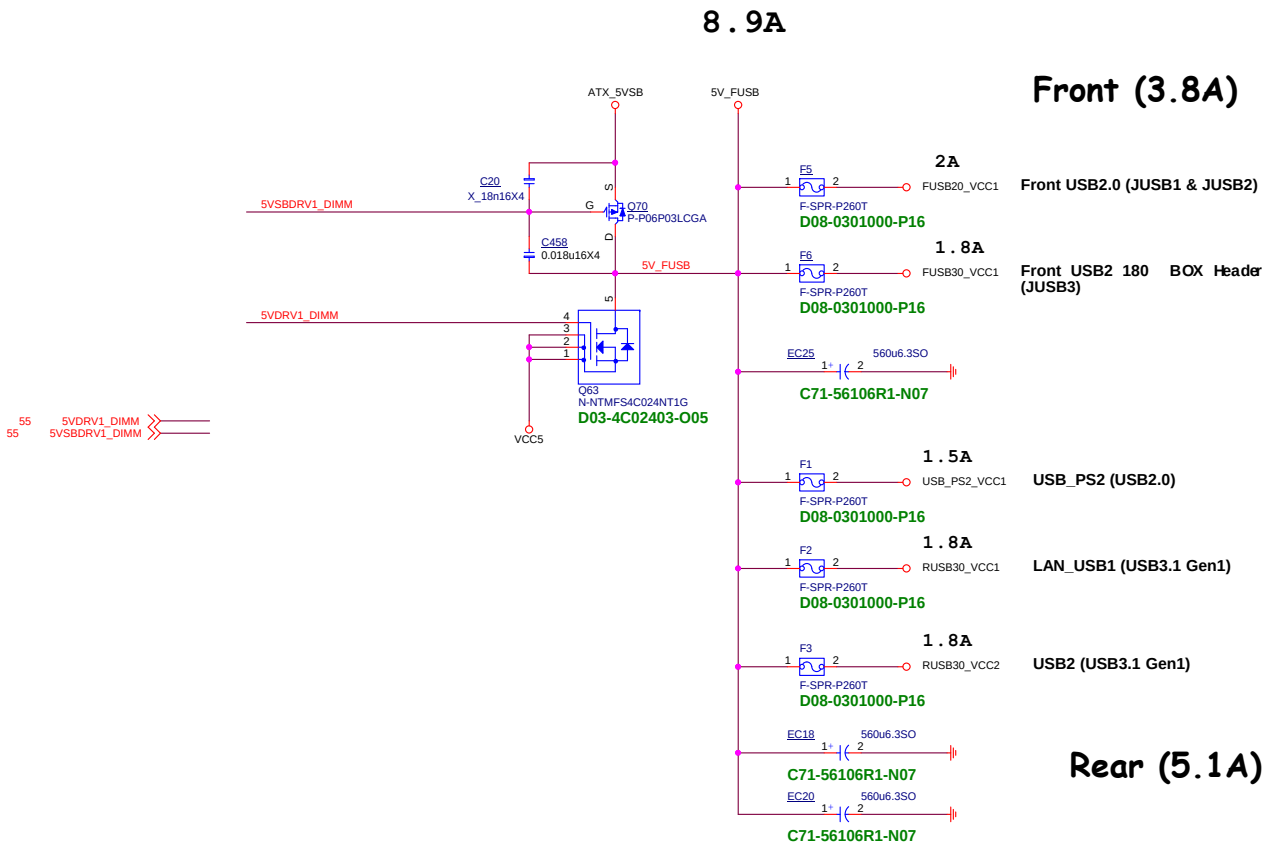
USB Power



MICRO-STAR INT'L CO.,LTD		
MS-7D14		
Size: Custom	Document Description: 34 USB Power - UP7501	Rev: 21
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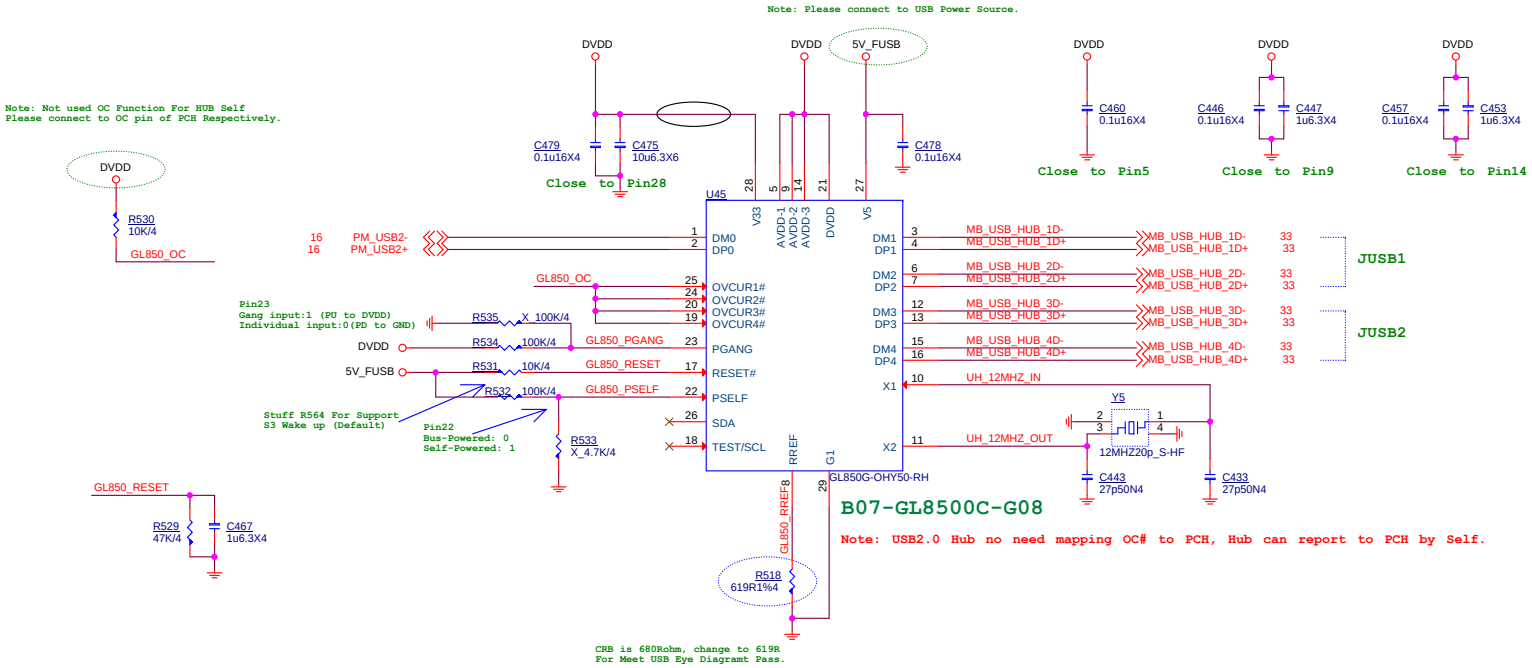
GL850G USB2.0 HUB



MICRO-STAR INT'L CO.,LTD		
MS-7D14		
Size: Custom	Document Description: 35 GL850G - USB2.0 HUB	Rev: 21
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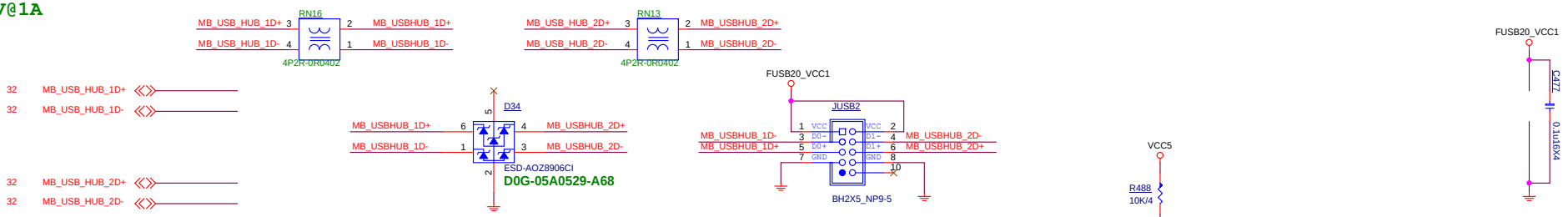
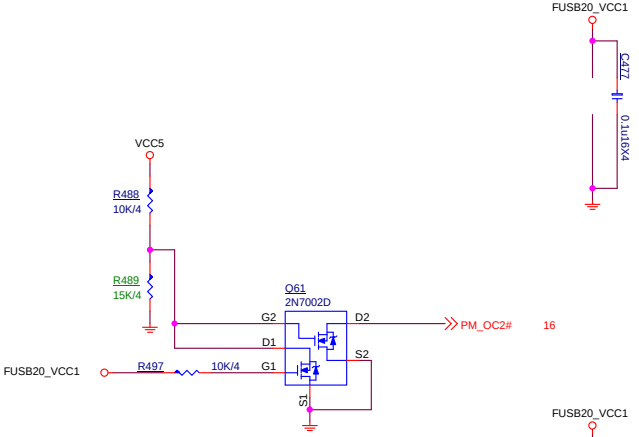
Front USB2.0(JUSB2)

Form GL850G USB2.0 HUB

5V@1A

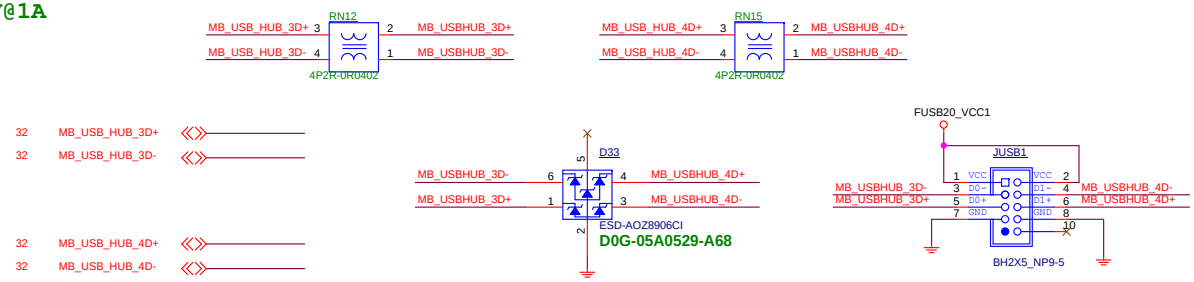


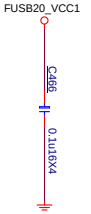


Front USB2.0(JUSB1)

Form GL850G USB2.0 HUB

5V@1A





MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: 36 Front USB2.0 Header	Rev: 21
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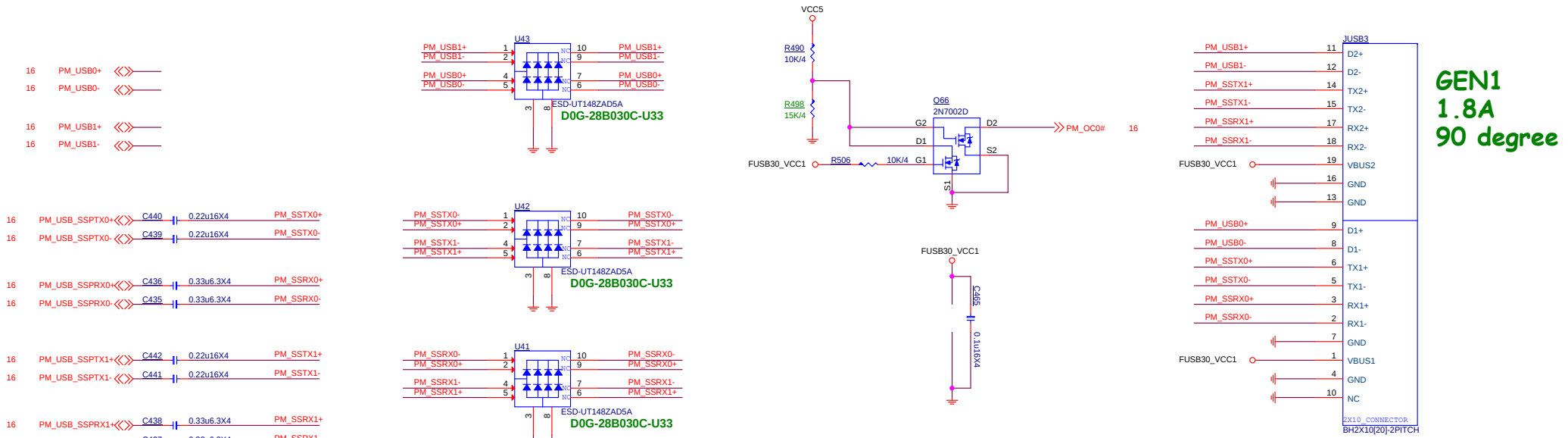

MICRO-STAR INT'L CO.,LTD			
MS-7D14			
Size: Custom	Document Description: 39 Front USB3.0 Header		Rev: 21
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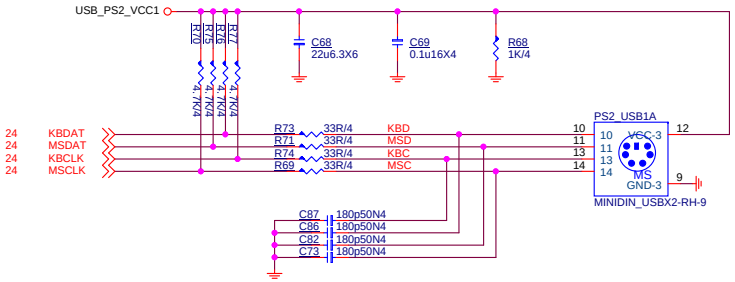
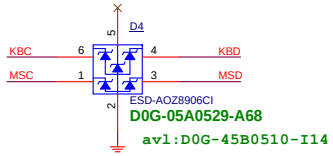
PS2+USB (USB2.0)

5V@0.5A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

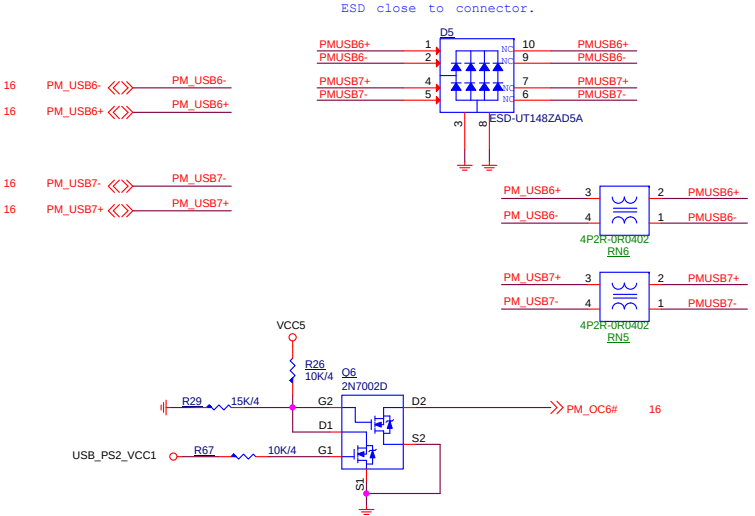


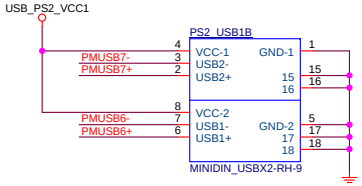


D0G-05A0529-A68

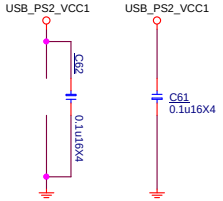
avl:D0G-45B0510-I14

ESD close to connector.





1A



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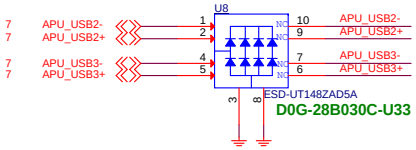
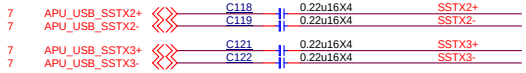
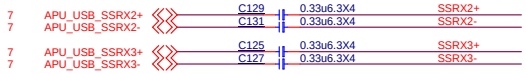
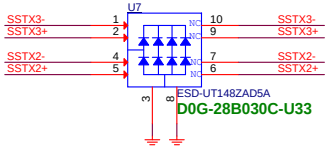
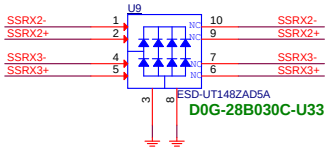
Rear USB3.2 GEN1 5V@1.8A

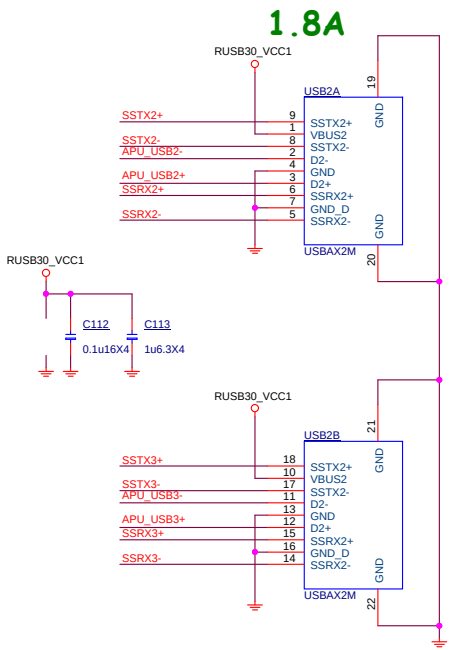












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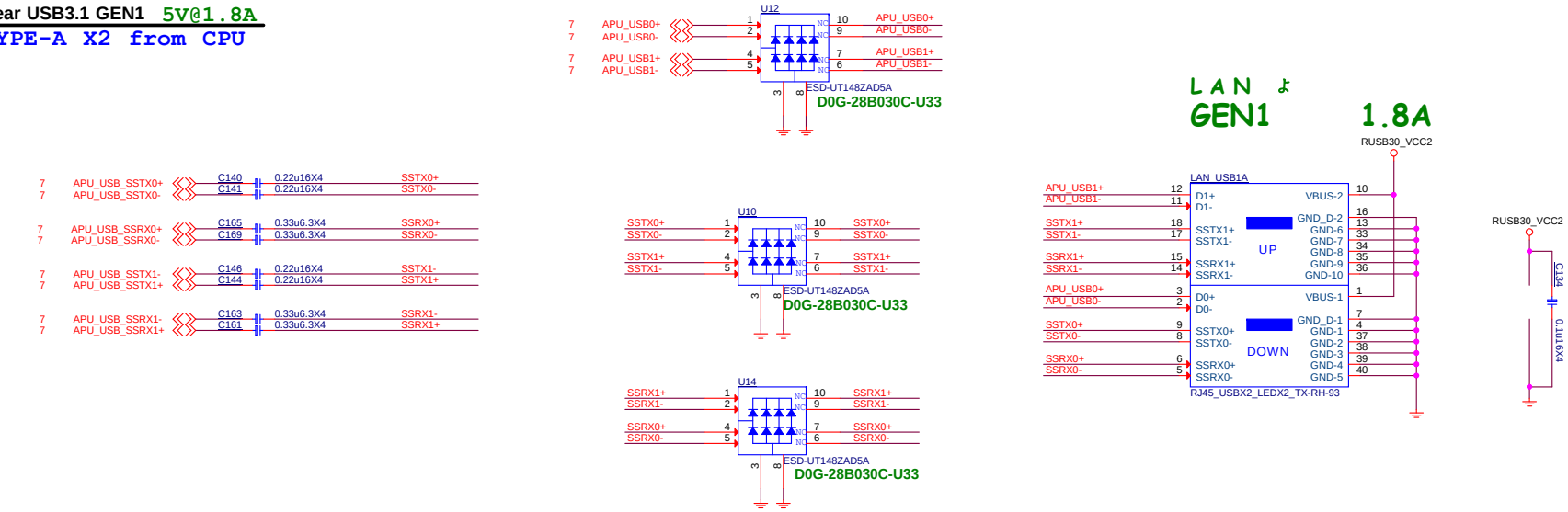
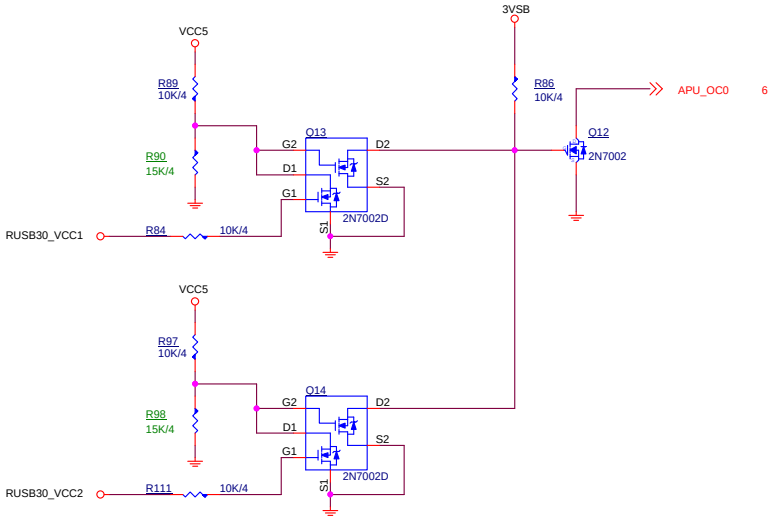
Rear USB3.1 GEN1 5V@1.8A

TYPE-A X2 from CPU



CPU OC Logic



Type1/2/3/4 High Active

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

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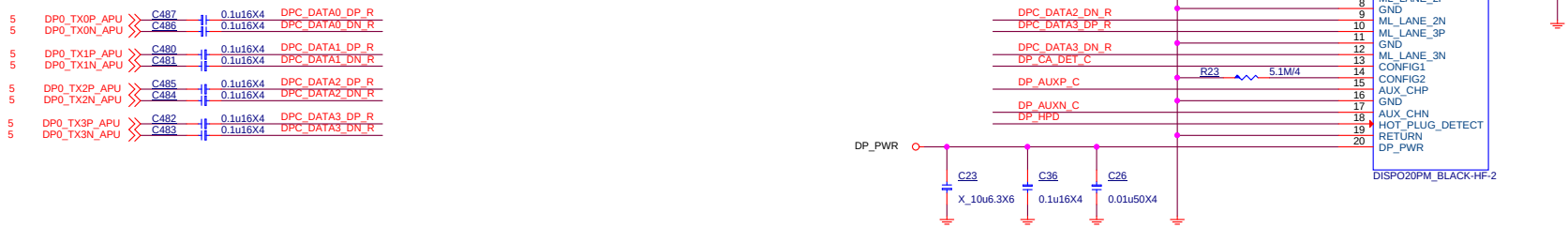
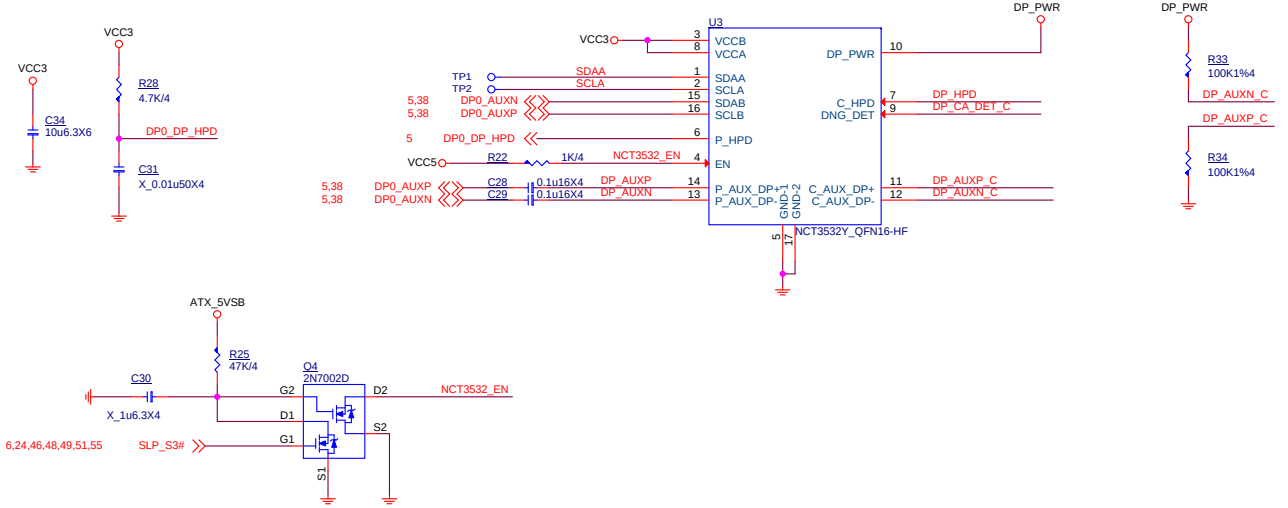
DP CONNECTOR

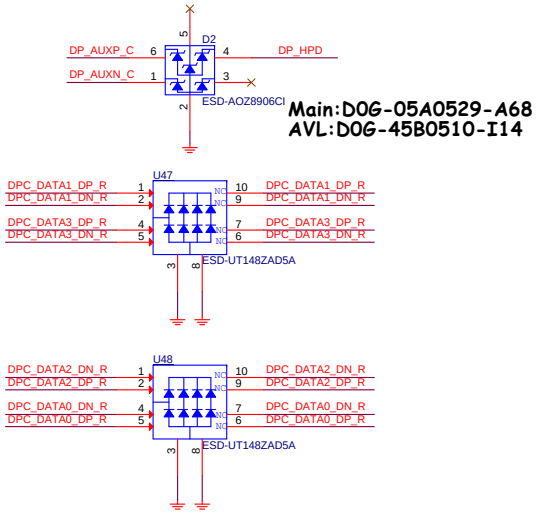


DP AUX & HPD Circuit

Support HDMI Dongle



ESD



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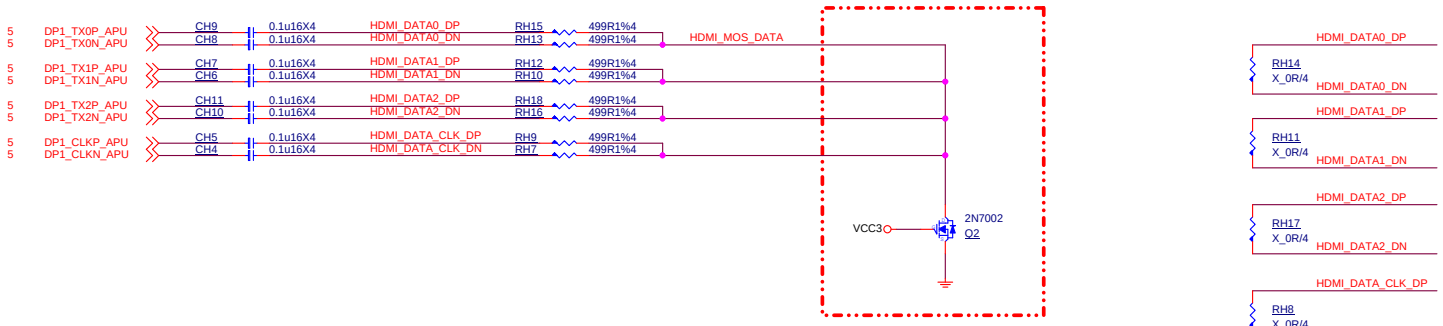
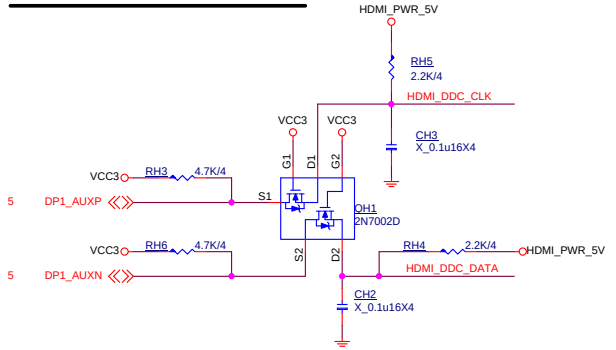
HDMI CONNECTOR

For HDMI 1.4

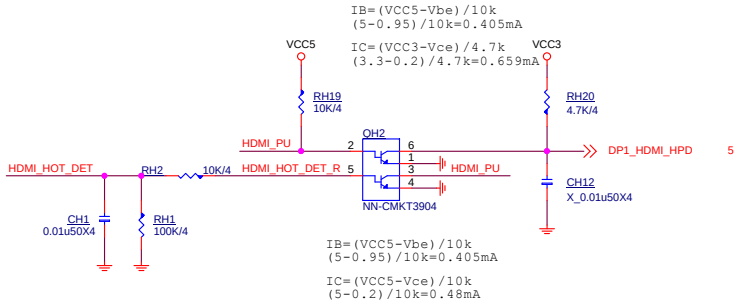


HDMI_MOS_DATA trace length <500mil
other platform please check design guide

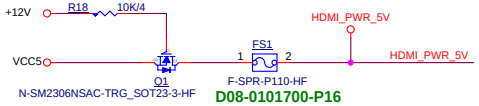
AUX Level Shifter



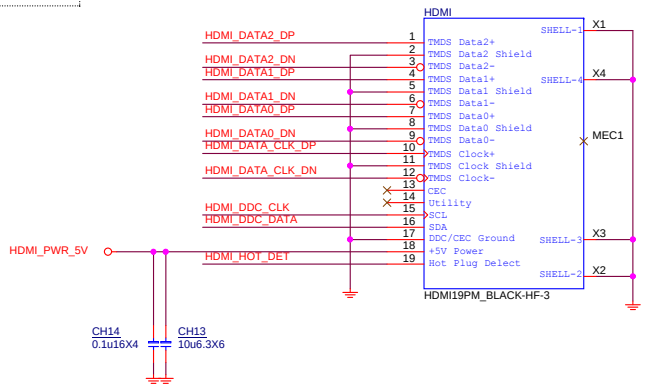
HPD Circuit



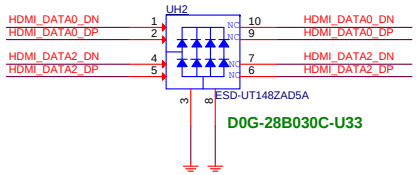
Connector Power

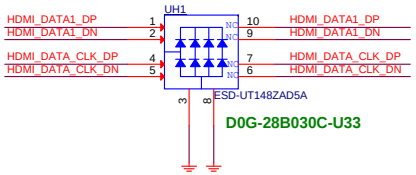


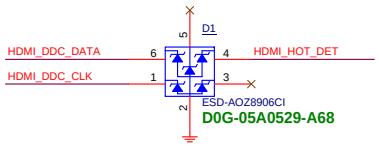
Connector



For EMI







MSI	MICRO-STAR INT'L CO.,LTD	
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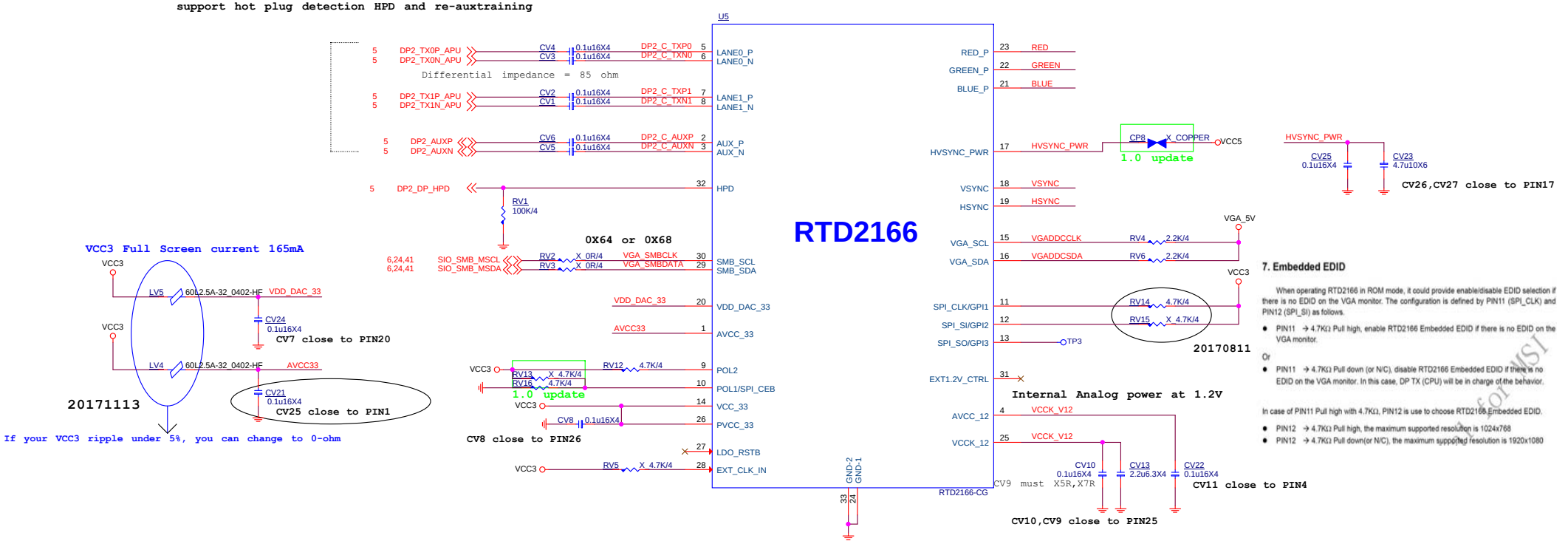
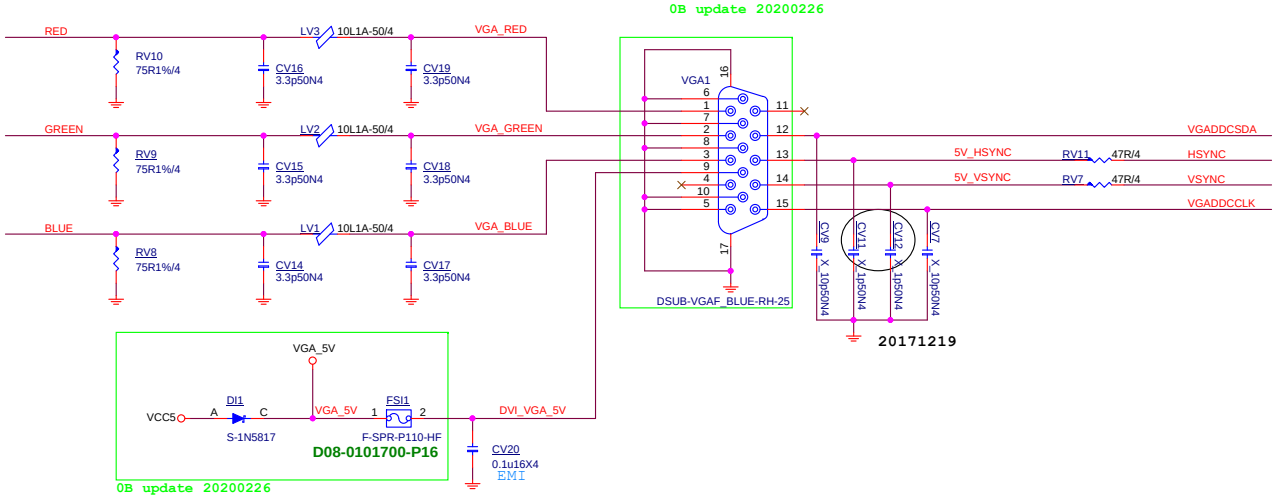
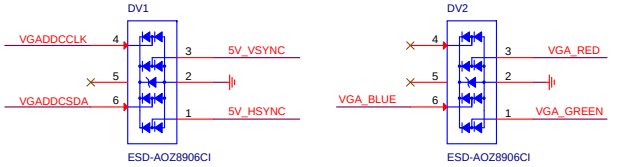
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining







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Vcore GROUP G TDC:95A,EDC:140A
NB GROUP C TDC:50A,EDC75A

Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

RT8894JGQW_WQFN56-HF

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation

VCORE IccMAX: 140A =>OCP=>180A (4 x 45A)
LL=1.3m ohm
VCC_NB IccMAX: 75A =>OCP=> 90A
LL 2.1m ohm
FSK:250K

1.0 update

VRHOT=150 degree, 115 degree reset
Close to PWM
Close to MOSFET

VRHOT=125 degree, 90 degree reset
Close to PWM
Close to MOSFET

close to PWM
close to phase1 CHOKE

close to PWM
close to phase1 CHOKE

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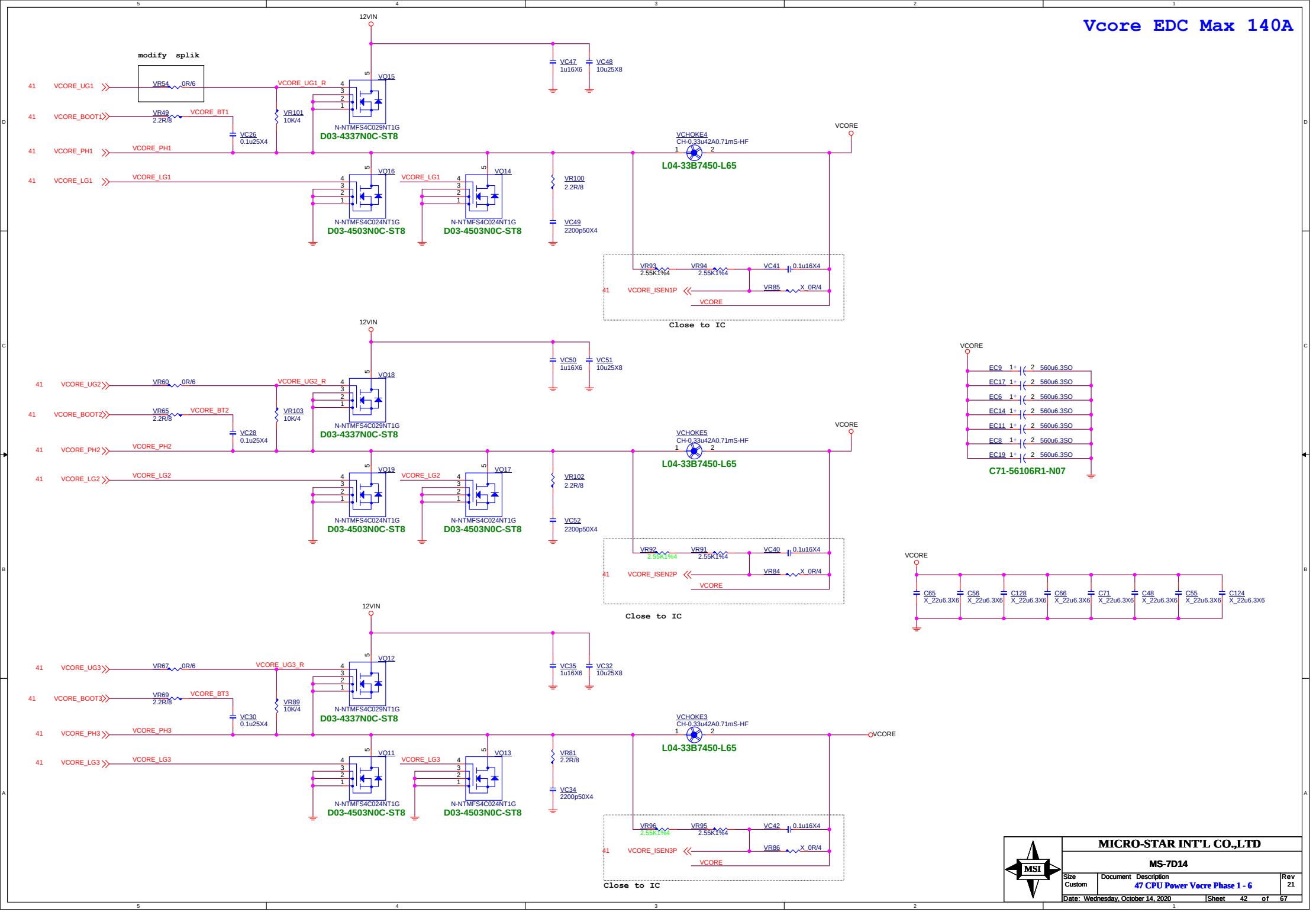
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD	
MS-7D14	
Size: Custom	Document Description: 47 CPU Power Vocre Phase 1 - 6
Rev: 21	
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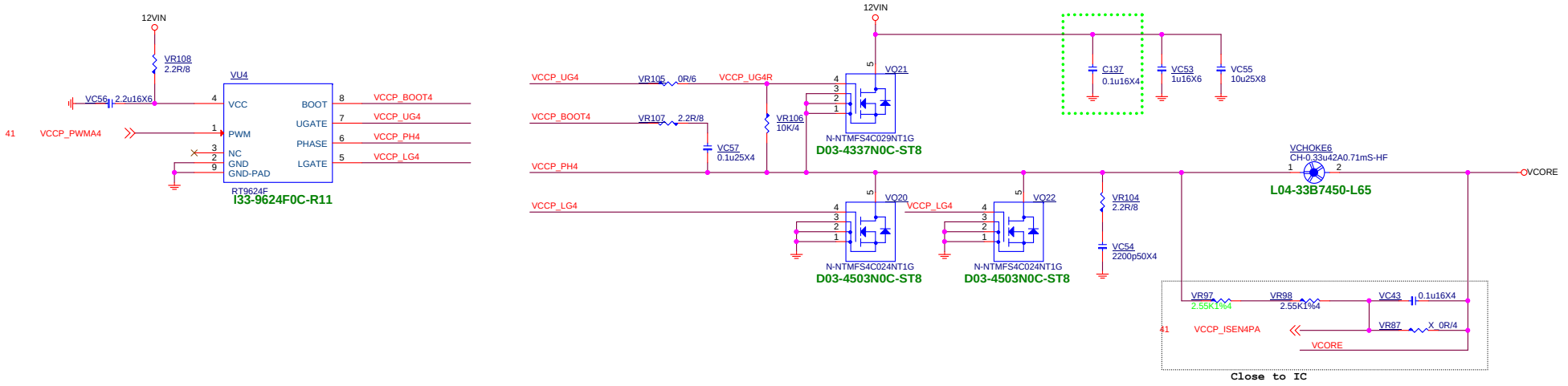

MICRO-STAR INT'L CO.,LTD		
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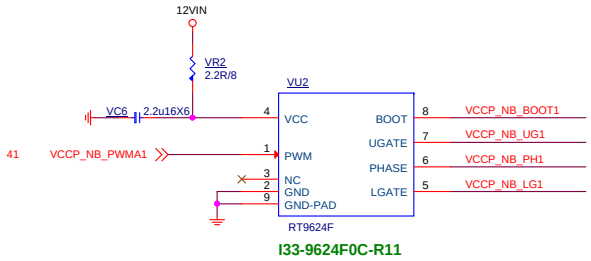
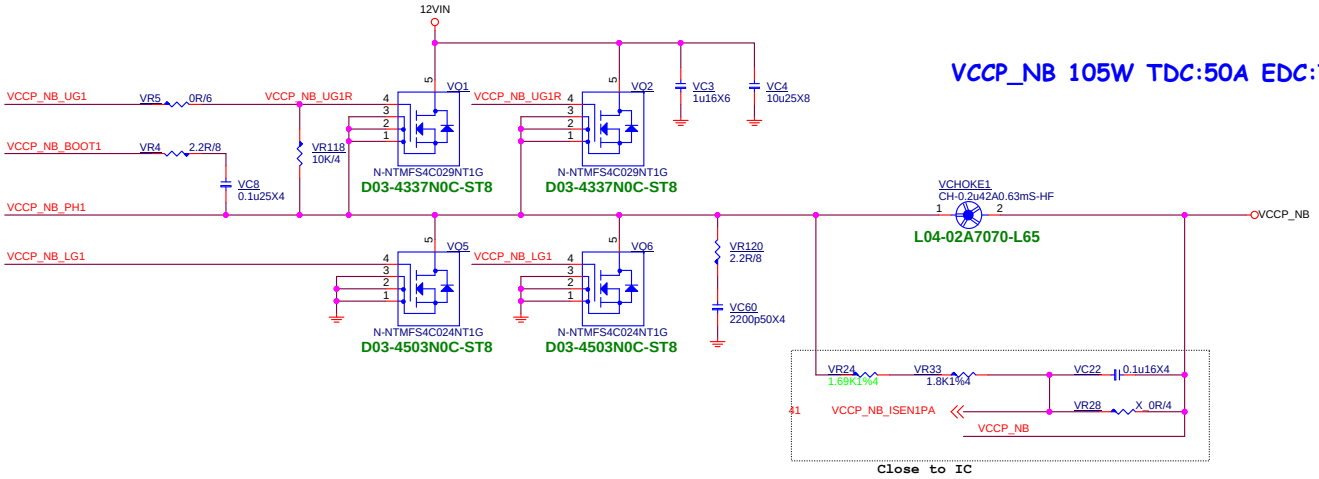
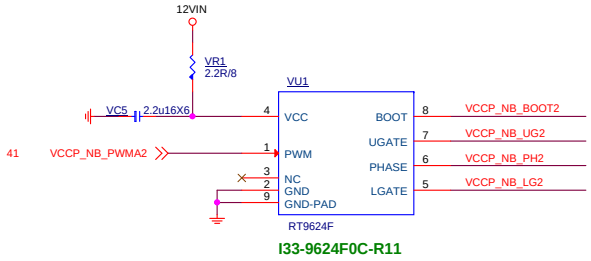
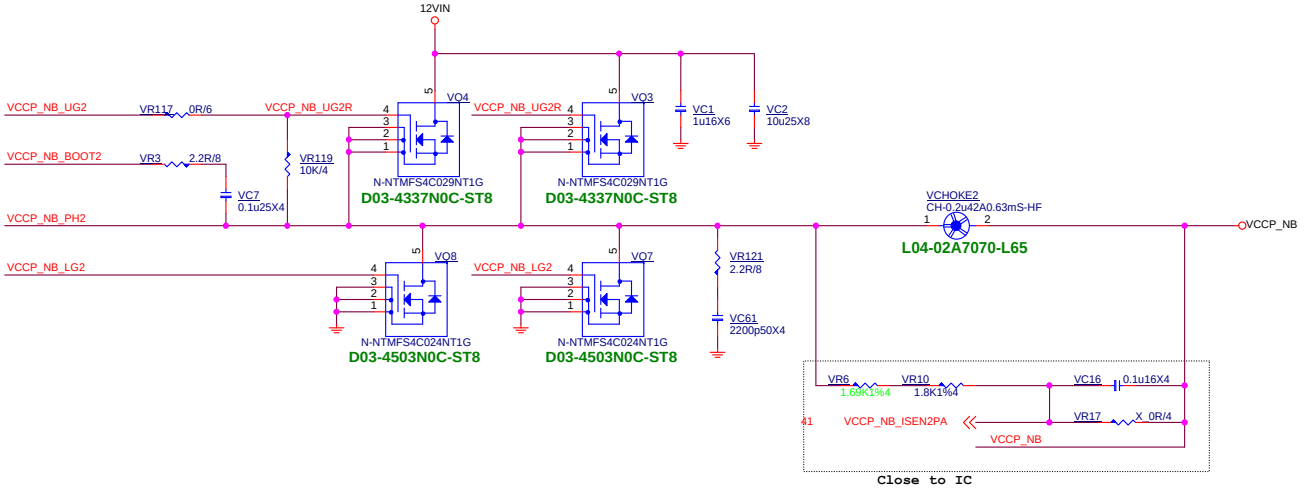
SOC EDC Max 75A

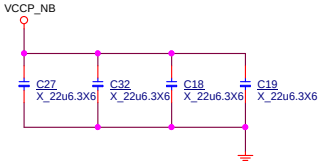
VCCP_NB 105W TDC:50A EDC:75A

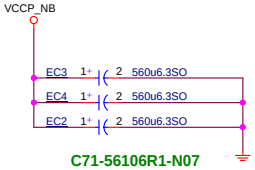












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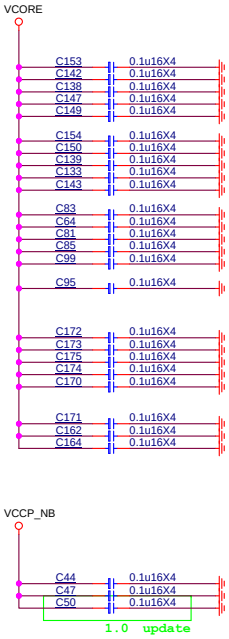

MICRO-STAR INT'L CO.,LTD		
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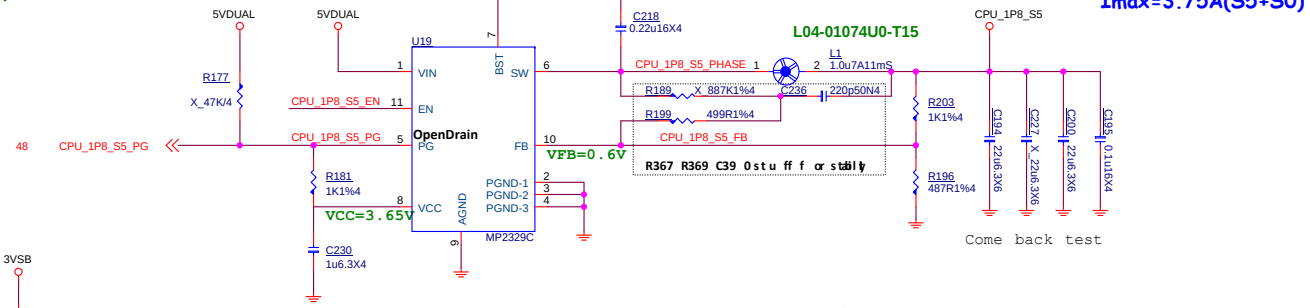
CPU 1.8V S5

CPU_1.8V △ 2A
CPU_VDDP_S5 △ 1A
VDD_1.8V_S5 △ 0.5A
AUDIO1.8V △ 0.25A

Continuous Conduction Mode (CCM)

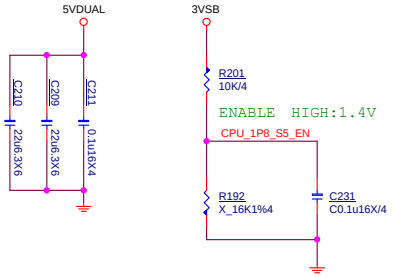
CPU_1P8_BST CPU_1P8_BST_R >50 mils.

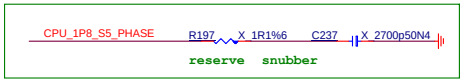
OCP:6.5A
Imax=3.75A(S5+S0)



I9C-2329C0C-M03
fix CCM mode

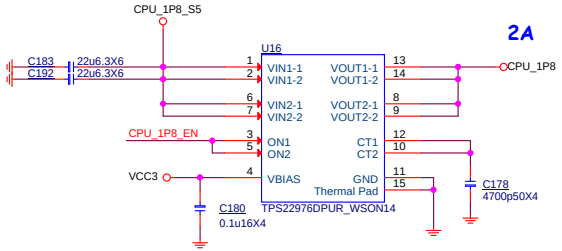
Vout = Vref * (1 +(R368/R372))
= 0.6 * (1 +(1K/487))
= 1.83V



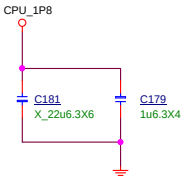


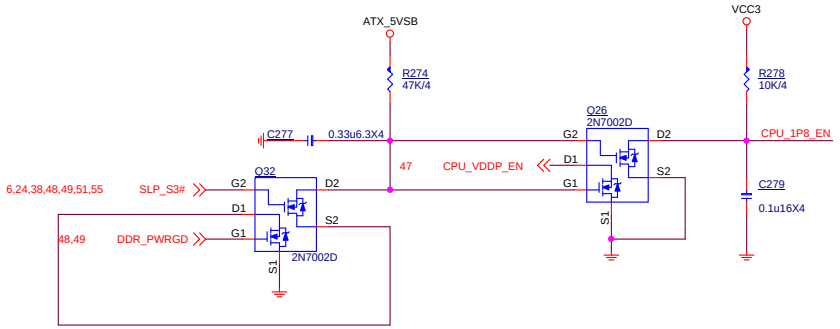
CPU 1.8V S0

CPU 1.8V_S0@2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (s/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in
(s/V)





DDR_PWRGD
CPU_VDDP
CPU_1P8

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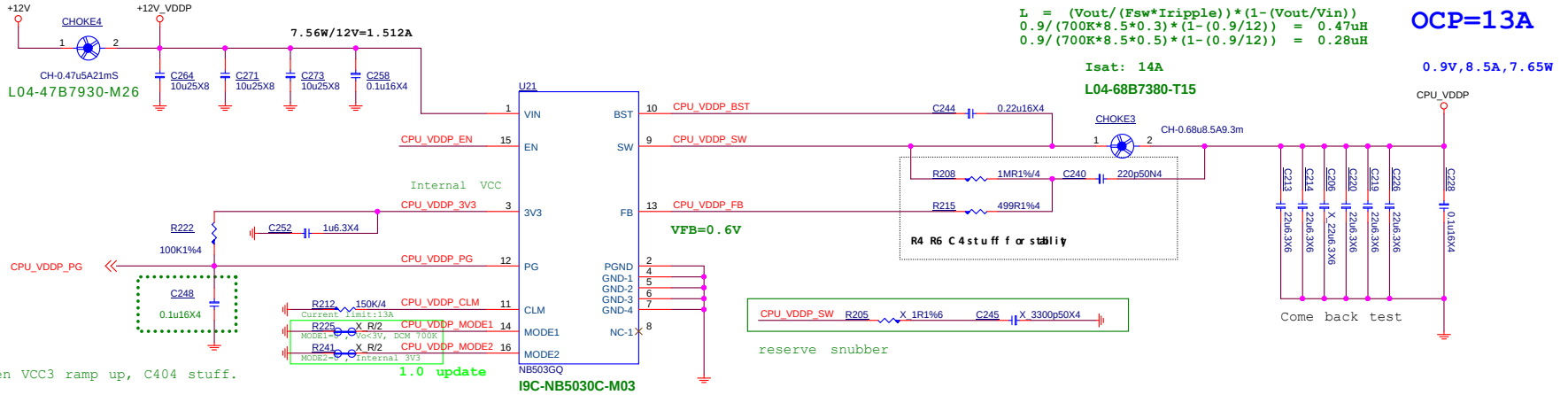
CPU_VDDP_S0

0.9V@S0:8.5A

S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```




```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
```

OCP=13A

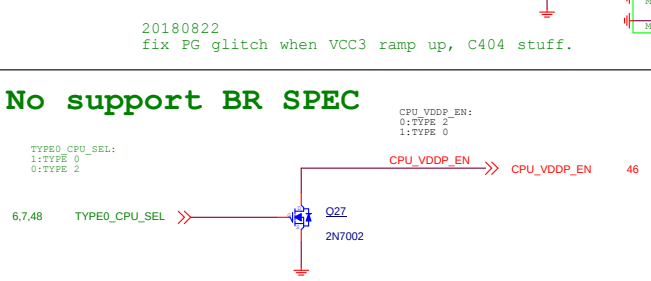
Isat: 14A

L04-68B7380-T15

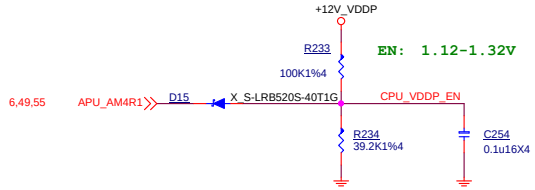
0.9V,8.5A,7.65W

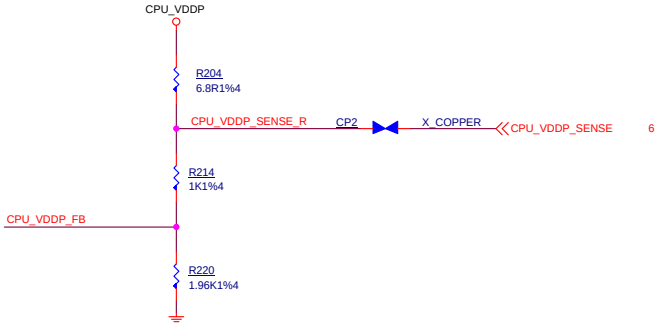
20180822
fix PG glitch when VCC3 ramp up, C404 stuff.

No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN	
BR	0	1	0	1	SPEC no Support
NA	X	0	0	0	
SR	2	1	1	0	NOT SUPPORT TYPE2
RV/ZP	3	0	1	1	
MTS	4	1	1	1	NOT SUPPORT TYPE4



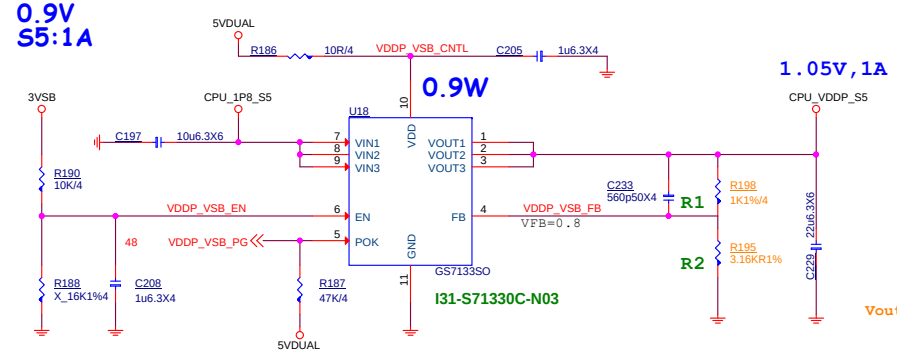



```
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
     = 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
     = 0.9058V
```

CPU_VDDP_S5

0.9V

S5:1A




```
Vout = Vref * (1+R489/R488)
     = 0.8 * (1+1K/3.16K)
     = 1.053v
```

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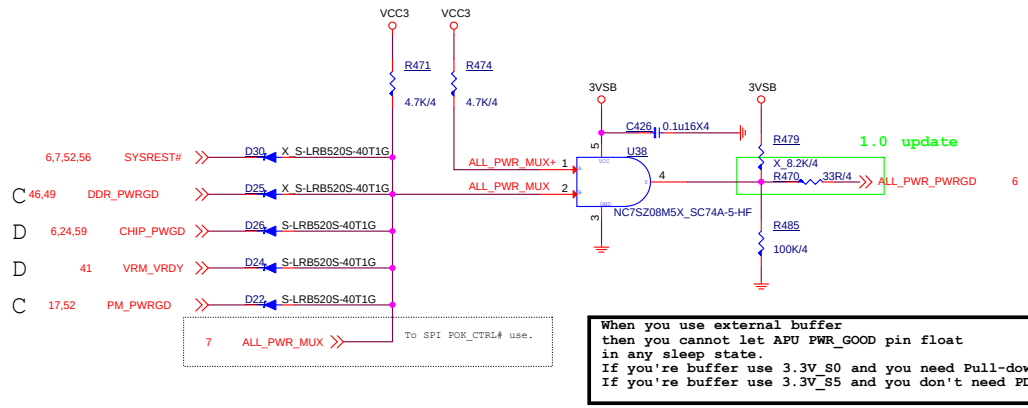
ALL POWER GOOD MUX

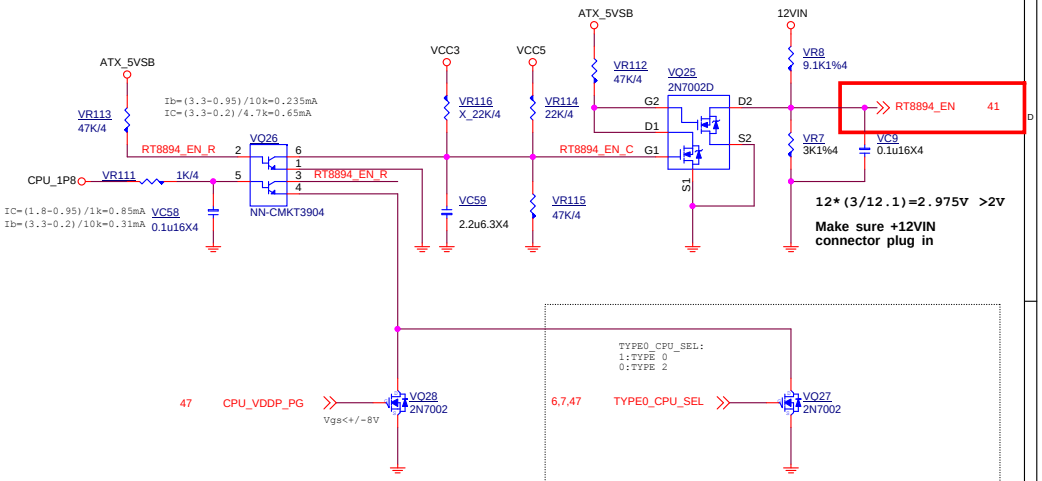
S0 PG



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit

1.0 update — remove D3



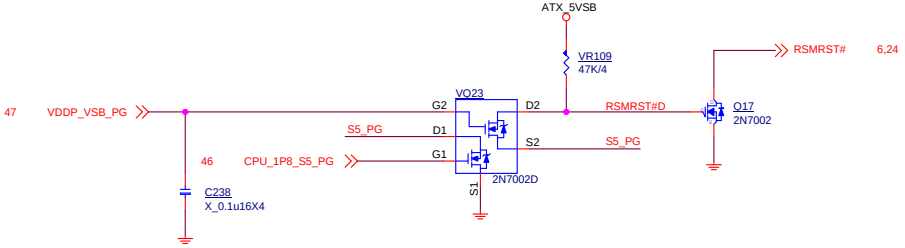
SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

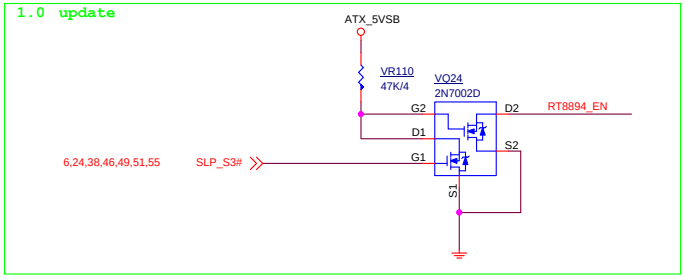
CPU VDDP NOT SUPPORT TYPE4

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1

S5 PG



1.0 update



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DDR4_1.2V
15.5A+4.75A+0.6A=20.85A
15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

OCP = 27.5A; Choke Isat=22A

Rocset = Iocp * Rdson(low) *10/ 5uA
= 27.5 * 5.1mohm *10/ 5uA
= 280.5K

Rdson(Low Side) 5V
D03-4503N0C-ST8:3.9 ~ 5.1mohm

VID	Reference Voltage (V)
H	0.675
L	0.75

5VDIMM
R60 100KR0402
DDR_PWRGD

5VDIMM
R59 5.1R1%/4
C45 1u6.3X/4
46,48 DDR_PWRGD
2V
f:400KHz
R61 620K1%/4
R65 280K1%/4
Rd(on)=5.1m, OCP:27.45A
U6
VID
VDD
CS
PGOOD
S5
S3
VDDQ
VLDOIN
VTTREF
VTT
VTTSNS
VTTGND
VTT LDO
TON
UGATE
BOOT
PHASE
LGATE
FB
PGND
GND
PGND-1
DDR_UG1
DDR_BOOT1
DDR_PH1
DDR_LG1
DDR_FB
FB:0.75V
RT8231AGQW
VDDQ_EN
6,24,38,46,48,51,55 SLP_S3#
VCC_DDR
C46 C3300p50X/4
VTT_DDR
C49 10u6.3X/6
C52 10u6.3X/6
Close to PIN19
VCC_DDR
C53 10u6.3X/6
CP1
X_COPPER
53 DDR_OV
DDR_OV
VCC_DDR
R47 0R1%/4 close to DIMM side
R62 1K1%/4
C43 X_68p10N/4
R48 1.65KR1%0402
R46 X_0R/4
C42 X_C0.1u16X0402
VDDIO_MEM_S3_SENSE 6
Default = 1.21V
I32-8231A0C-R11

5VDIMM
CHOKE1 CH-0.22u8A9m
C22 1u6.3X/4
C17 X_1u6.3X/4
EC5 CD560M6.3SQ-HF-5
C38 C0.1u16X0402
C37 C22u6.3X/6
C40 C22u6.3X/6
C41 C22u6.3X/6
5VDIMM_IN
5VDIMM_IN

24 SIO_VDDQ_EN
R385 X_R/2
R222 remove
1.0 update
ATX_5VSB
R255 47K/4
Q21 2N7002D
6,47,55 APU_AM4R1
ATX_5VSB
R275 X_47K/4
Q24 X_2N7002D
6,24,51,55 SLP_S5#
VDDQ_EN
1.0 update

Irms = Iout * SQRT[(Vout/Vin) * (1 - (Vout/Vin))]
= 28.7* SQRT[(1.2/5*(1-(1.2/5))]
= 11.15A

5VDIMM_IN
DDR_UG1
DDR_BOOT1
DDR_PH1
DDR_LG1
Q10
N-SM4337NSKPC-TRG_DFN5x6-8-HF
D03-4337N0C-ST8
Q11
N-SM4503NHKPC-TRG_DFN5x6-8-HF
D03-4503N0C-ST8
C51 C0.1u25X0402-HF
R66 X_1R1%
C59 X_C3300p50X/4
CHOKE2 CH-0.47u22A1.8m
EC13 CD560M6.3SQ-HF-5
EC15 CD560M6.3SQ-HF-5
C70 C0.1u16X0402
VCC_DDR
Imax:20.85A
1.2V
0.1uFx1 per dimm
VTT_DDR
C107 X_C0.1u16X0402
C109 X_C0.1u16X0402
VCC_DDR
C111
VTT_DDR
C0.22u16X0402-HF

UPI VOLTAGE CONSOLE

2019/4/30
EC18, EC19 are changed to C71-56106K1-AO5
by PM spec updated.

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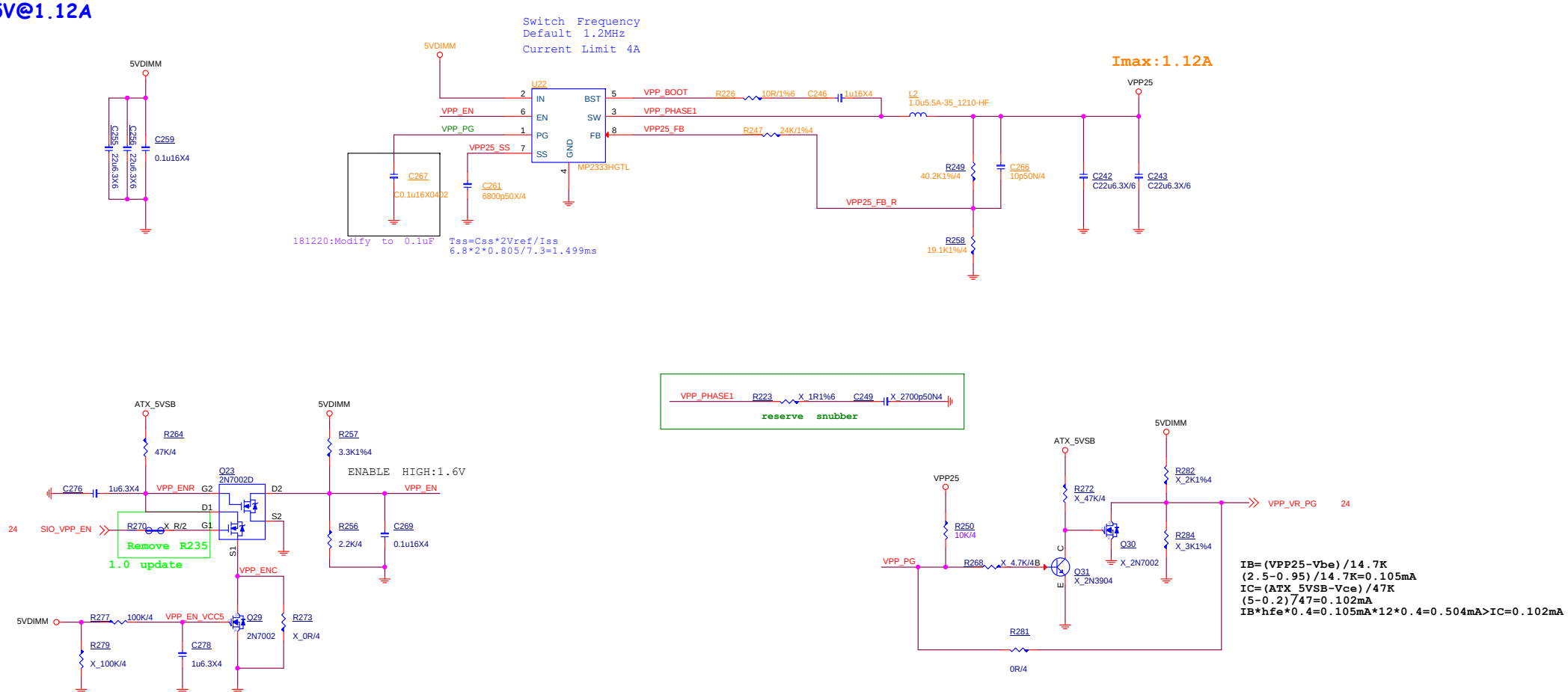
2DIMM : VPP25

2.5V@1.12A



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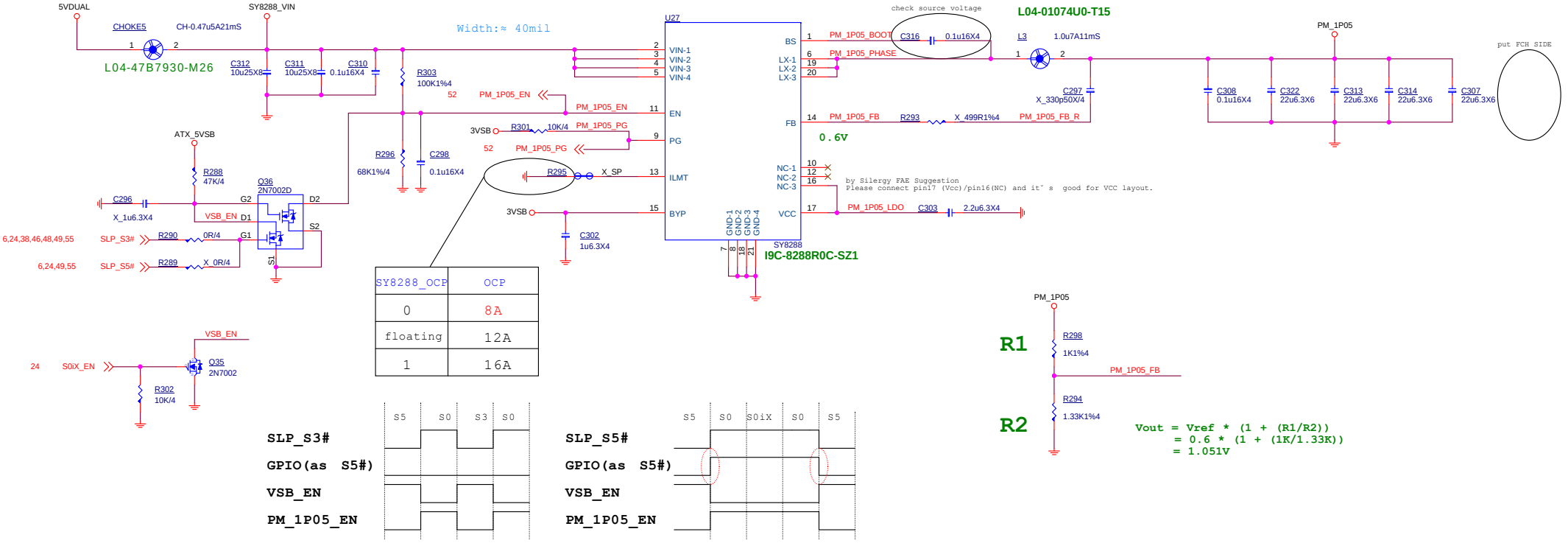
FOR Promontory 1.05V_S0

1.05V
S0:5.5A

Input Current= (8A*1.05V)/5V/0.85=1.976A

OCP=8A

1.05V@5.5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051V

FOR PROM PM_1P05_S5

1.05V@0.05A

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MS-7D14			
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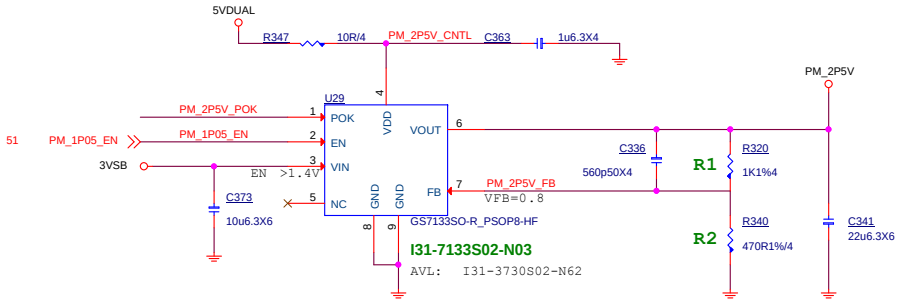
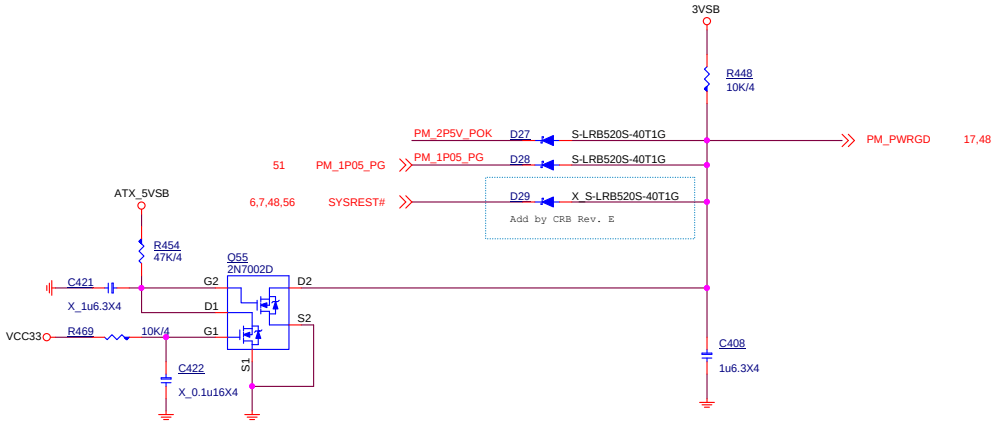
Promontory-2.5V

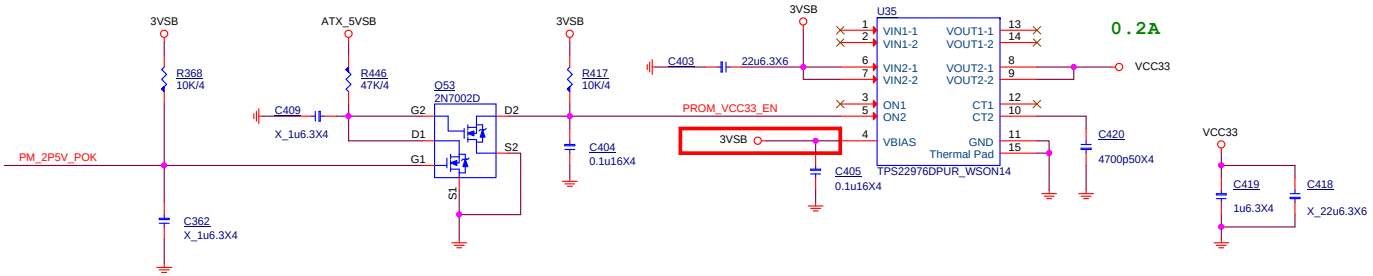
2.5V@900mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/0.47K))
= 2.502V



VCC33 VCC33@0.2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (s/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in
(s/V)

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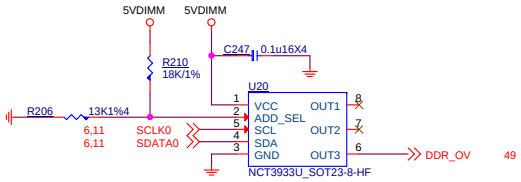
Over Voltage Control IC

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

0x26:RH=18K,RL=13K



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MS-7D14		
Size: Custom	Document Description: 58 OV Control - NCT3933	Rev: 21
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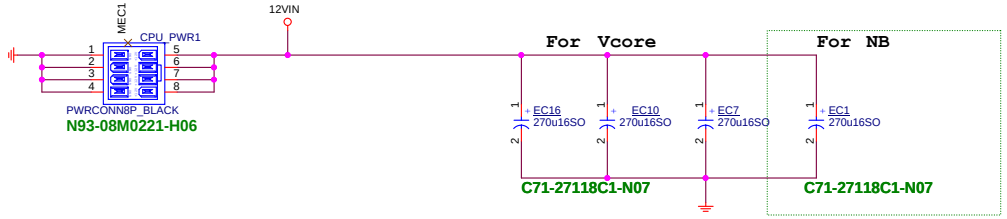
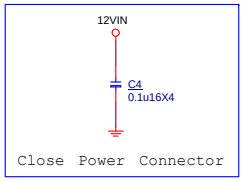
CPU POWER CONNECTOR



Vcore			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	
I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	10	phase
I ripple	=	5.962848	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

SOC			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.



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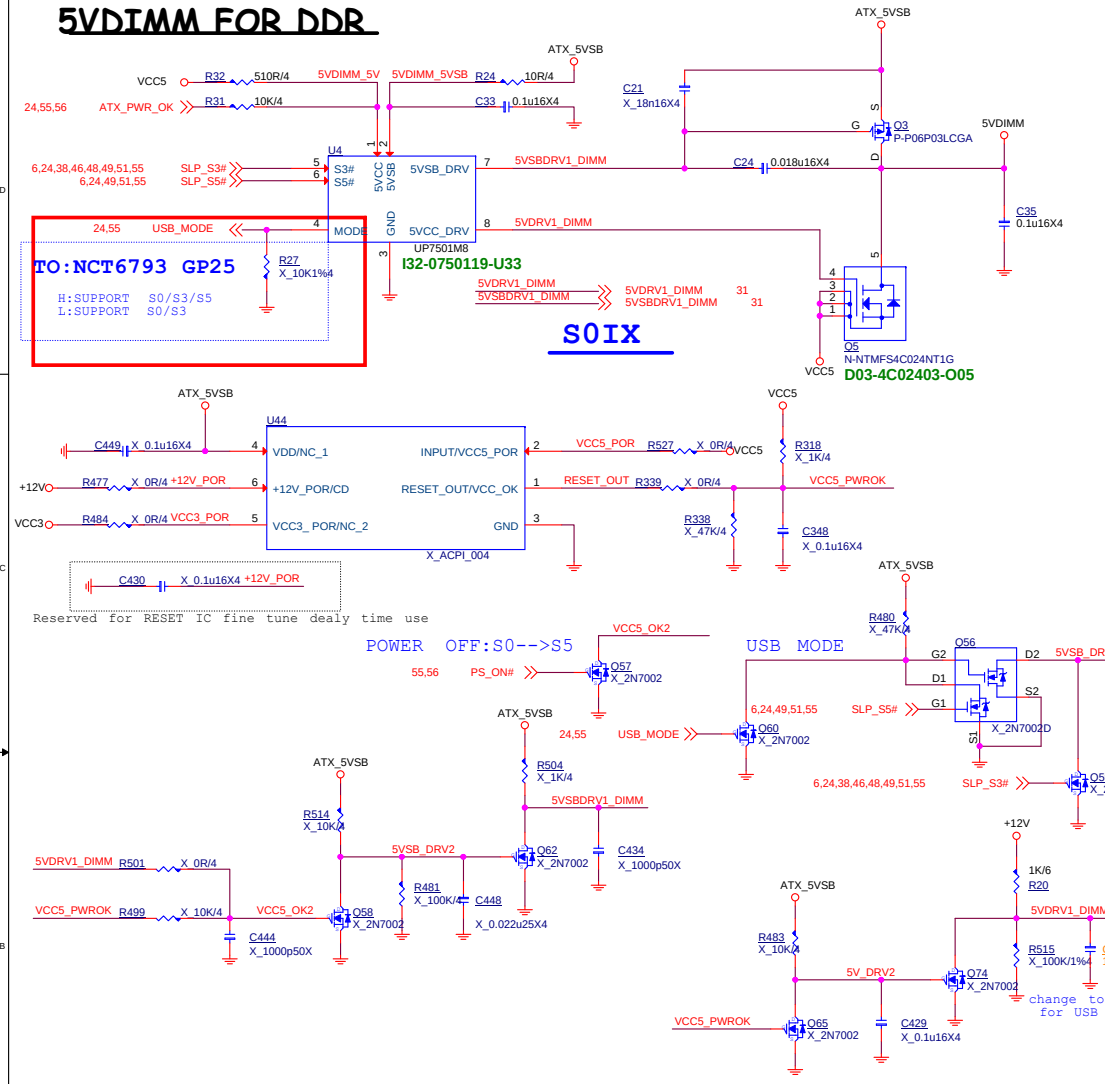
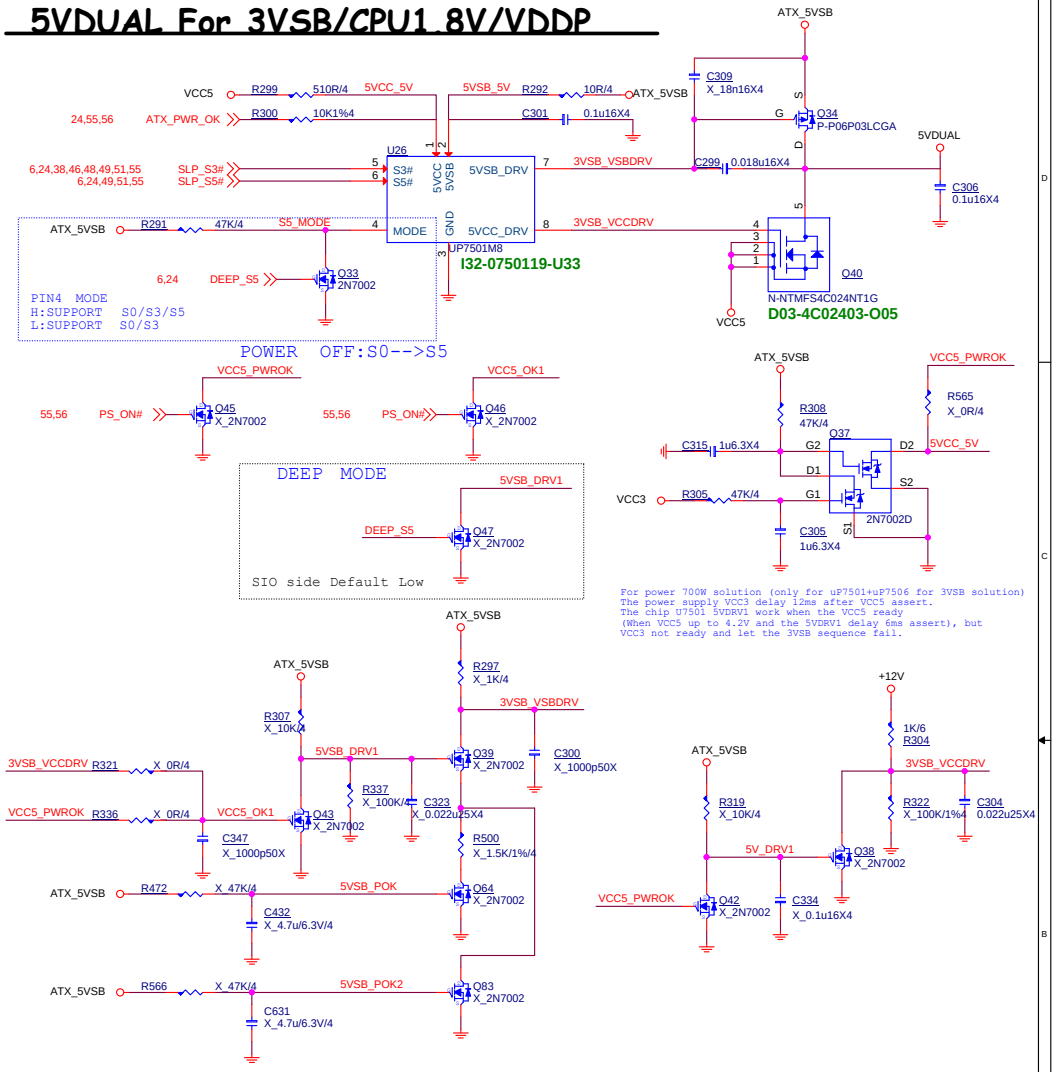
5VDIMM FOR DDR



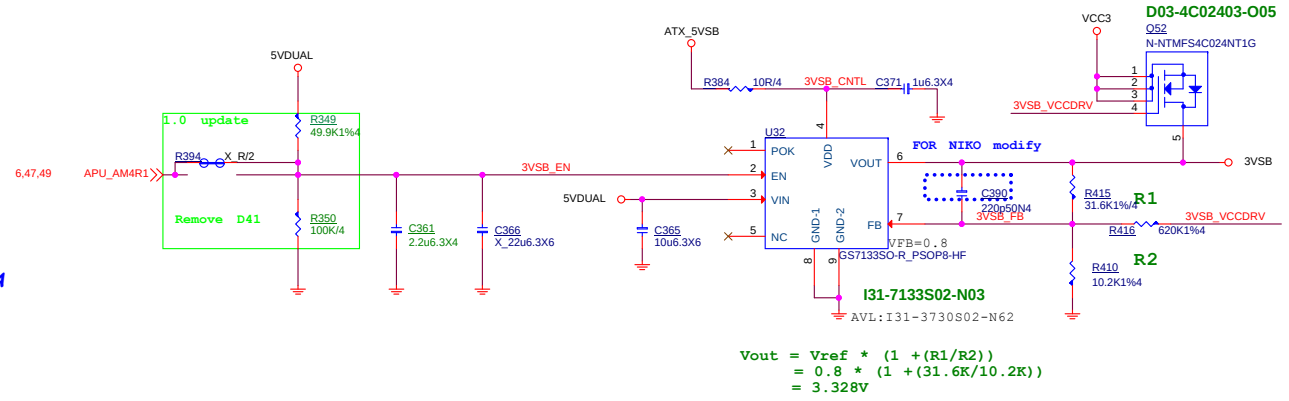
5VDUAL For 3VSB/CPU1.8V/VDDP



3VSB cost down

3.3V@1.61A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.1A
*PCIE=(375mA*1+0.02*2)=0.415A*
M.2WIFI= 0.78A
RTL8111H=0.065A



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

MICRO-STAR INT'L CO.,LTD

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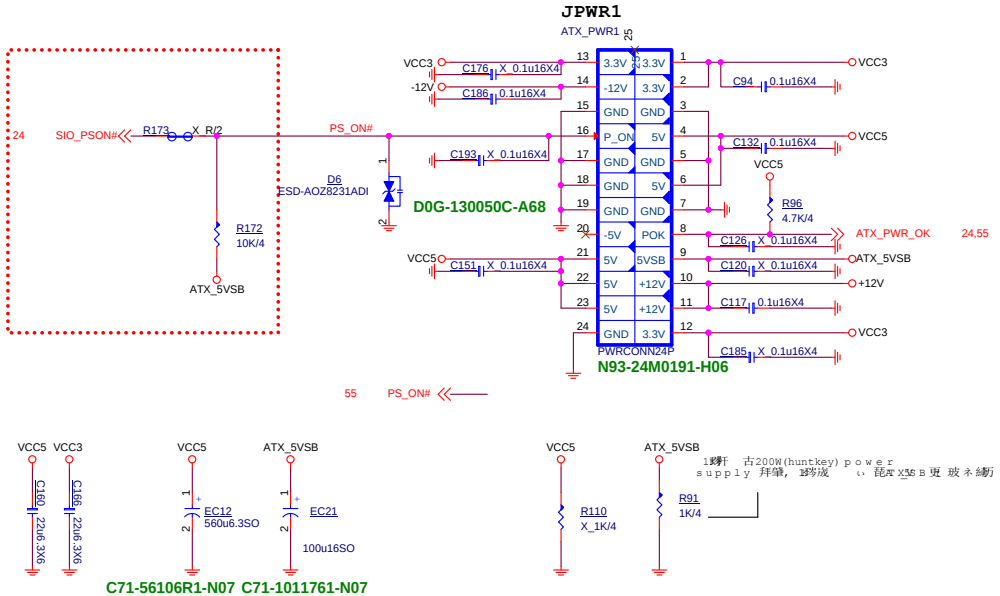
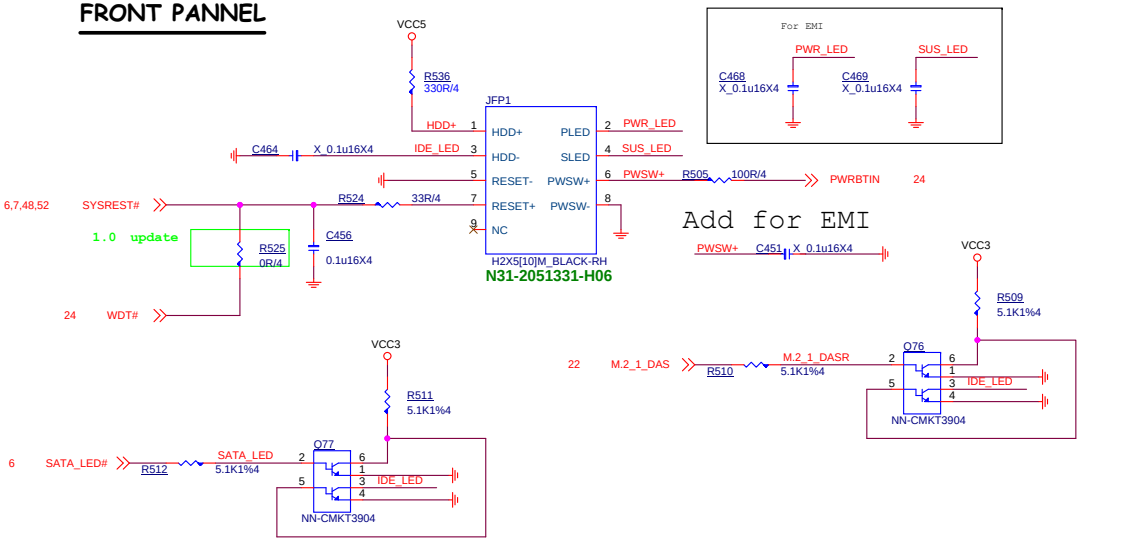
ATX POWER CONNECTOR

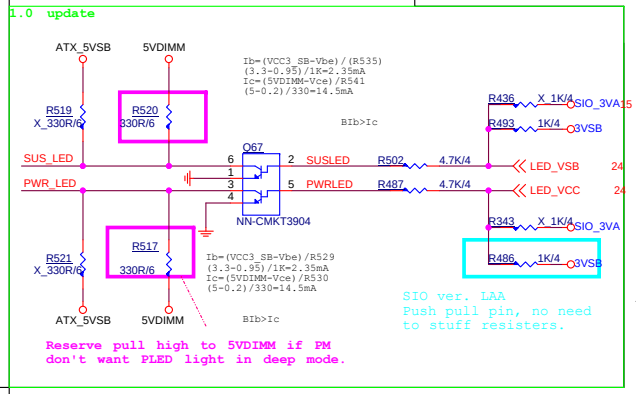


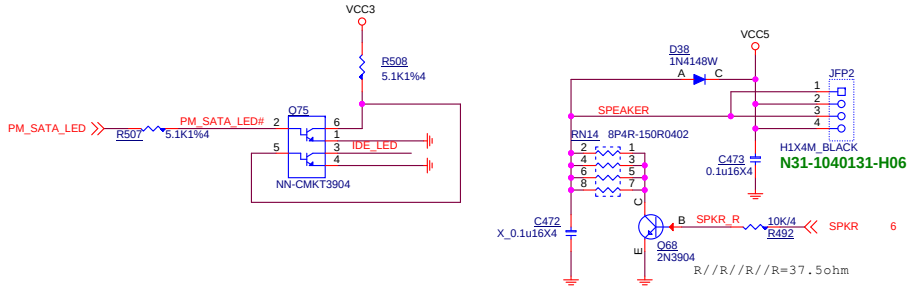
FRONT PANNEL



TPM

LED (for ESIO)





Voltage Mearsure Point

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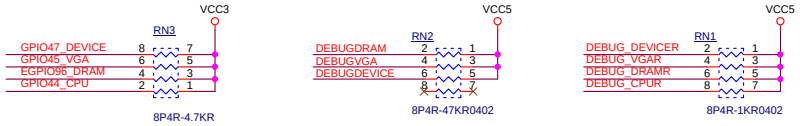
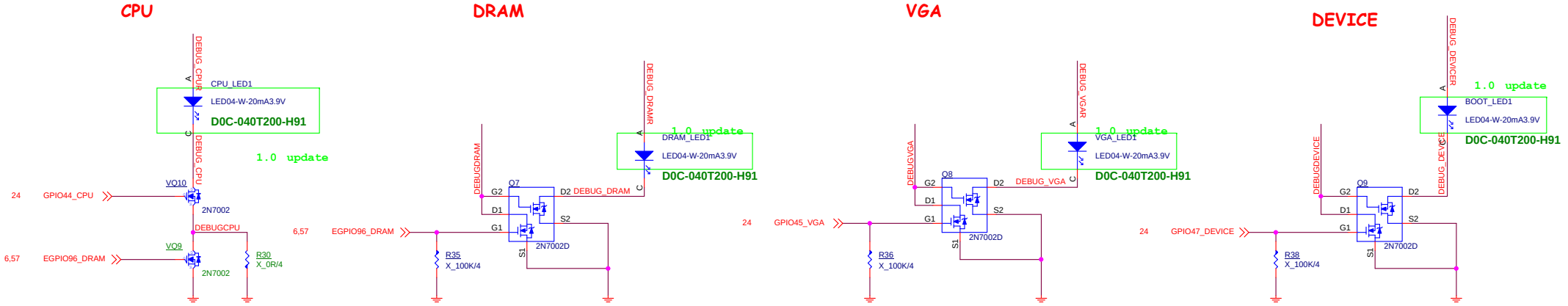
EZ Debug LED





LEDGPIO	GPIO46	EGPIO96	GPIO44	GPIO13
獵	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
陋	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

LED 獵 蝻 豔 C 即 L 画 奔

DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07

AMD AMP Detect LED

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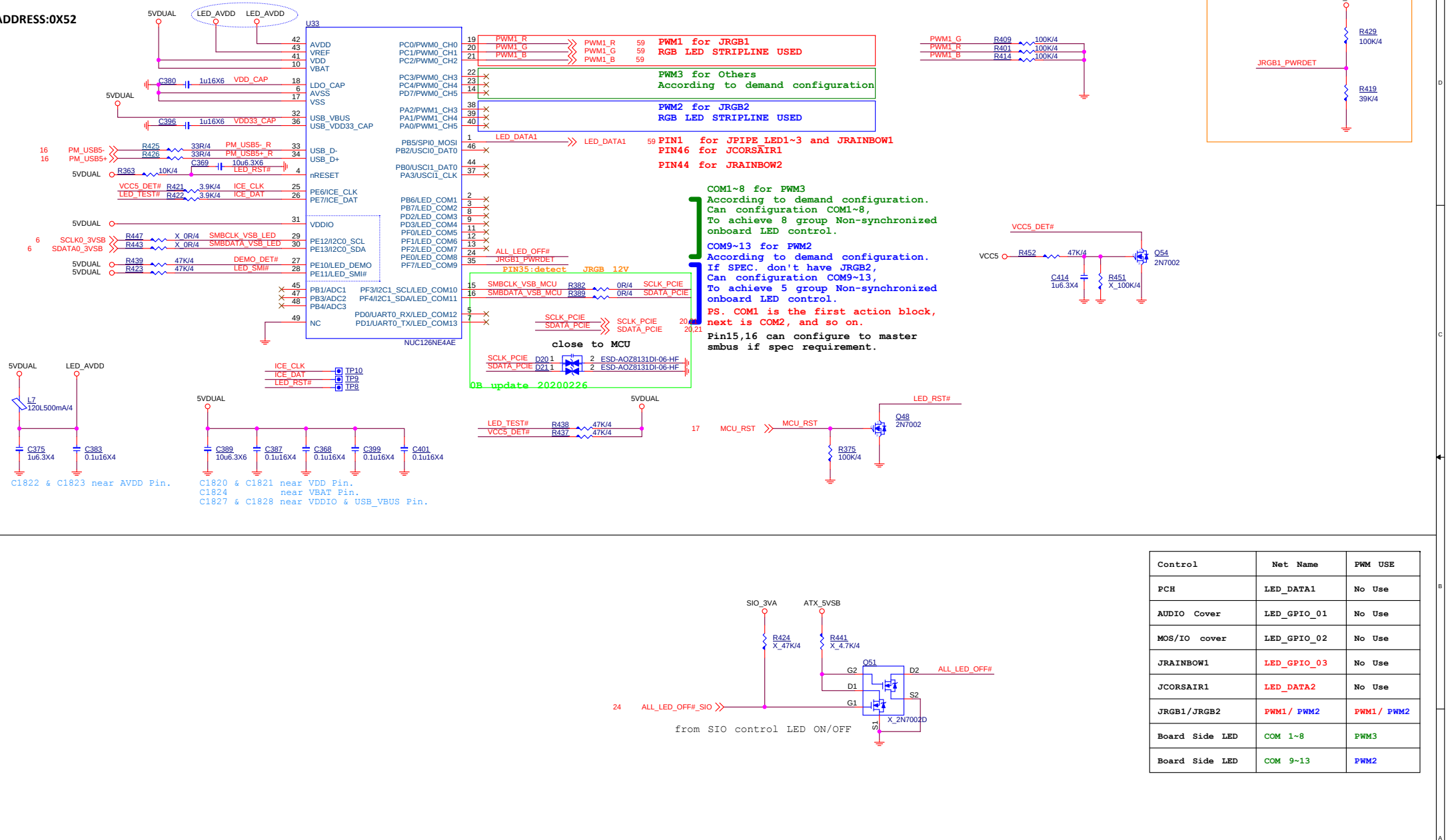
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

MICRO-STAR INT'L CO.,LTD

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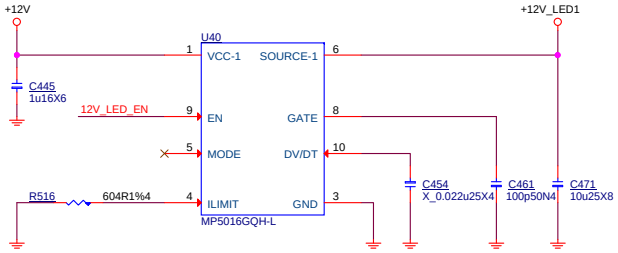
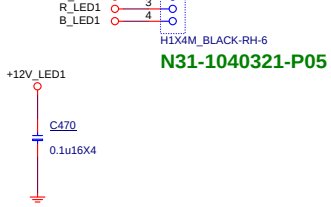
JRGB1

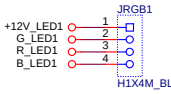
Trip@3.6A

>60mil

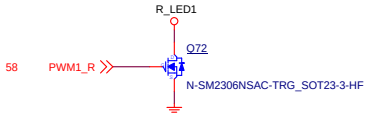
>60mil

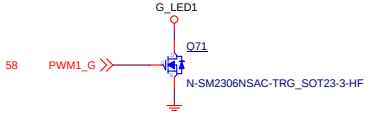


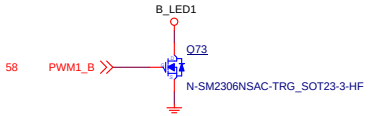


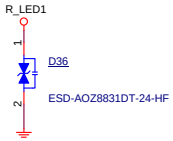


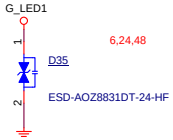
N31-1040321-P05

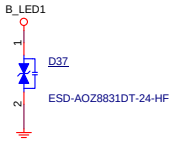


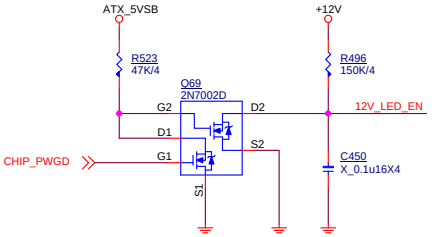






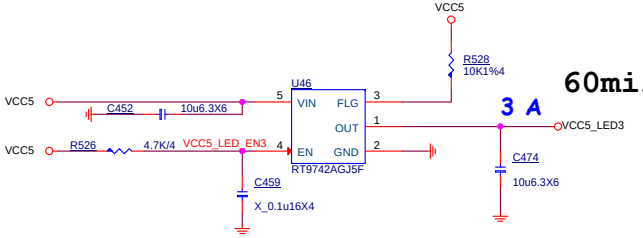


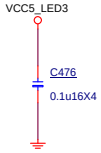


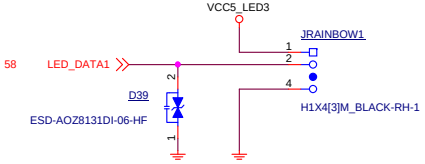


JRAINBOW1

60mil







JCORSAIR1

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Size: Custom	Document Description: 64 LED - JRGB1/2 JRAINBO1/2	Rev: 21
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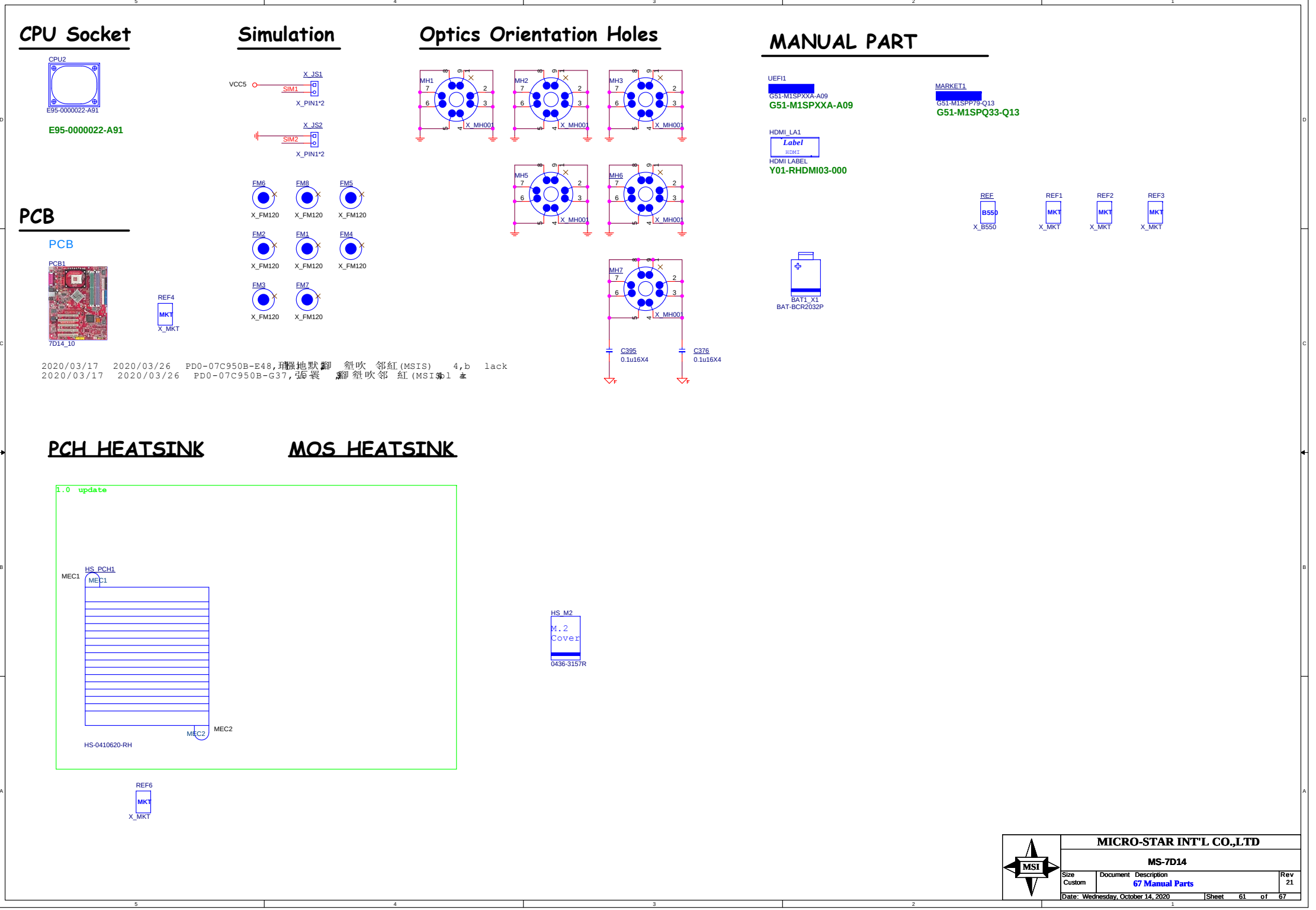
MS-7D14	
Size: Custom	Document Description: 66 BOM Option
Rev: 21	
Date: Wednesday, October 14, 2020	Sheet 60 of 67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MH5
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MH7
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C376
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MOS HEATSINK
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MEC2
HS-0410620-RH
HS_M2
M.2
Cover
0436-3157R
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MKT
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67 Manual Parts
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